15th - 17th MAY 2024

Athens (Greece)

10th International EuroSOI Workshop and International Conference on Ultramate Integration on Silicon

(EuroSOI-ULIS) 2024

ABSTRACT BOOK

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Preface

It is a great pleasure to welcome you to the 10th Joint EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS 2024), 15-17 May 2024, Glyfada, Attica, Greece.

The Joint EuroSOI-ULIS International Conference is an annual event running since 2013. The recent past 6 conferences in this series were organized in Athens, GR (2017), Granada, ES (2018), Grenoble, FR (2019), Caen, FR (virtual, 2020), Caen, FR (2021), Udine, IT (2022), Tarragona, ES (2023).

This Conference aims at gathering together in an interactive forum all scientists and engineers working in the field of SOI technology and advanced microelectronics devices. One of the key objectives of the conference is to promote collaboration and partnership between different academia, research and industry players in the field.

The conference venue is Oasis Hotel Apartments, a real oasis of leisure and relaxation by the sea, which is located in Glyfada, a cosmopolitan suburb of Athens Riviera.

We invite students and researchers from academic and industrial era working in topics related to conference's topics to submit their abstracts and to travel to Athens to attend the conference, meet their fellow colleagues, and enjoy this marvelous city.

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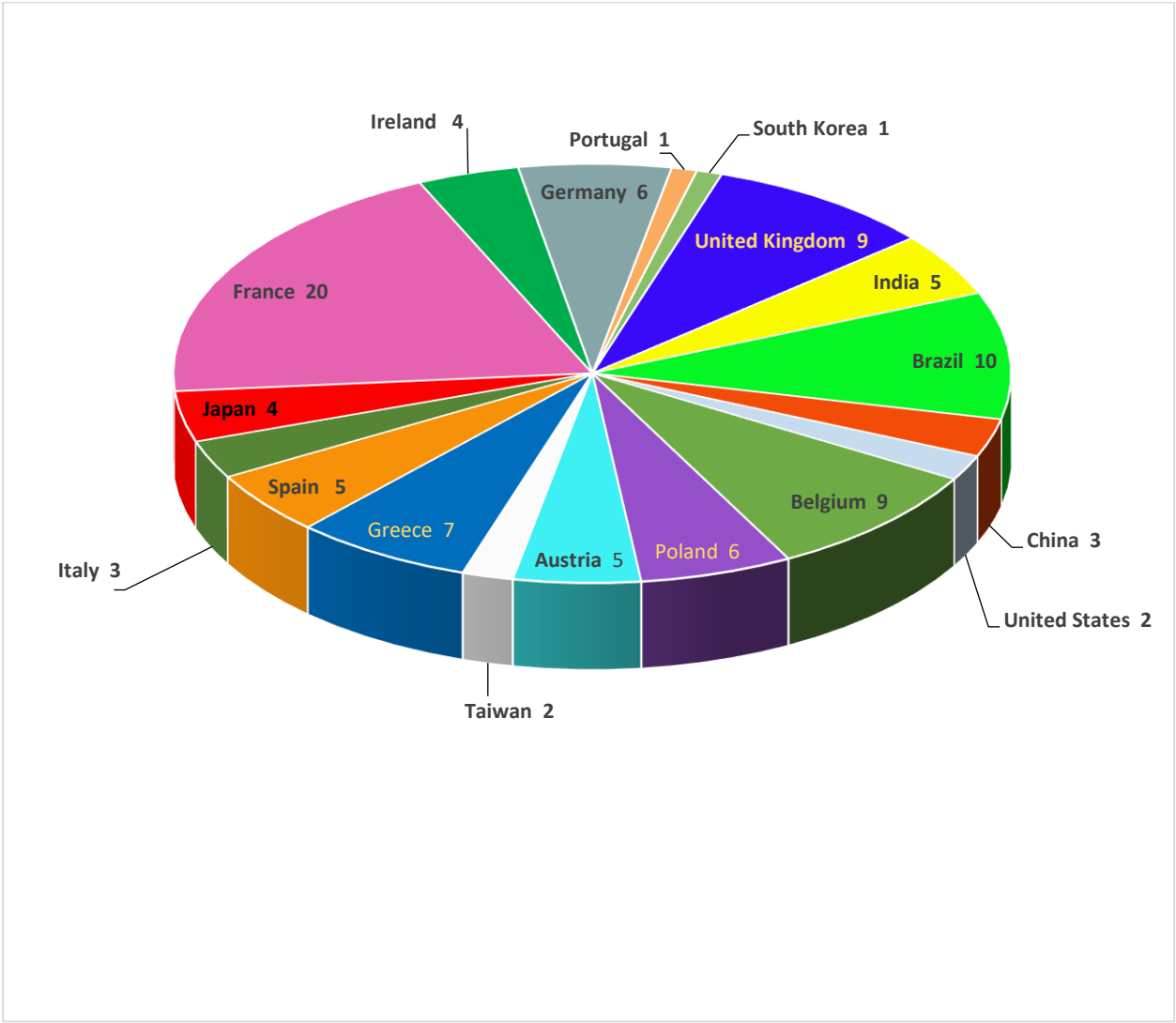
Conference Statistics



Participants: 102

France	20	Spain	5
Brazil	10	Ireland	4
Belgium	9	Japan	4
United Kingdom	9	China	3
Greece	7	Italy	3
Germany	6	Taiwan	2
Poland	6	United States	2
Austria	5	Portugal	1
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Oral Presentation

Enhanced Threshold Voltage Tuning in SOI MOSFET with Ferro-BOX

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Embedded in the gate stack, ferroelectric materials are of massive interest for the development of emerging sharp-switching transistor and non-volatile memory [1-2]. SOI devices feature an additional dielectric layer, the buried oxide (BOX), which can also be replaced by a ferroelectric for enriched functionality (Fig. 1a). HfO_2-based ferroelectric buried oxides (Fe-BOX) were fabricated in Popov's group and tested with the Pseudo-MOSFET method [3]. The polarization switch gives rise to two distinct non-volatile memory states.

Here, we explore a different avenue, that is the polarization-enhanced tuning of the threshold voltage in FD-SOI MOSFETs [4]. The interface coupling effect is arguably a most valuable asset of ultrathin FD-SOI technology, unheard of in FinFETs or nanowires. The rate of change of the threshold voltage with back-gate bias, derived from the equivalent circuit (Fig. 1b), is $\Delta V_T/\Delta V_{BG} = - t_{ox}/t_{box}$ [5]. The large difference between the thicknesses of the gate oxide ($t_{ox} \leqslant 1$ nm) and BOX ($t_{box} = 25$ nm) limits the tunability rate to 4%. Our aim is to amplify the tuning through a polarization mechanism in a Fe-BOX.

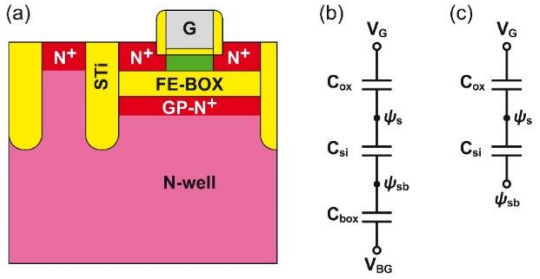

Fig. 1. (a) FD-SOI MOSFET with Ferro-BOX and equivalent circuit in subthreshold region for (b) regular BOX or (c) ferroelectric BOX.

The leading idea is to have V_{BG} acting directly on the back-surface potential ψ_{sb} at the film-BOX interface, without being absorbed by the thick BOX. This simplifies the equivalent circuit (Fig. 1c) and augments the tunability rate: $\Delta V_T/\Delta\psi_{sb} \approx - 3t_{ox}/t_{si}$. In the ideal case where V_{BG} is transferred integrally via the polarization effect ($\Delta V_{BG} = \Delta\psi_{sb}$), the rate of change reaches 50% for 1 nm EOT and 6 nm thick silicon body.

Proof-of-concept simulations were performed with Synopsis tools. The n-channel MOSFET structure (Fig. 1a) comprises a gate stack with 2 nm equivalent oxide thickness, a 7 nm thick undoped body, a 10 nm thick hafnium–zirconium oxide (HZO) BOX, and raised source and drain. The gate length, the doping of the ground plane and the programming pulse applied on the back gate are variable parameters. A remanent polarization of 40 $\mu C/cm^2$ and a coercive field of 1.5 MV/cm are considered.

Figure 2a shows that even with a modest program voltage, a remarkable V_T lowering is achieved. The V_T shift reaches 1 V after 1.5 V pulse. This performance is to be compared with only 60 mV shift for a regular 25 nm BOX. For effectiveness, the ground-plane should be heavily doped ($N_D > 2x10^{19}$ cm^{-3}), otherwise the series resistance absorbs part of the impulse (Fig. 2a). The initial value of the threshold voltage is recovered with a negative pulse (-6 V in Fig. 2b),

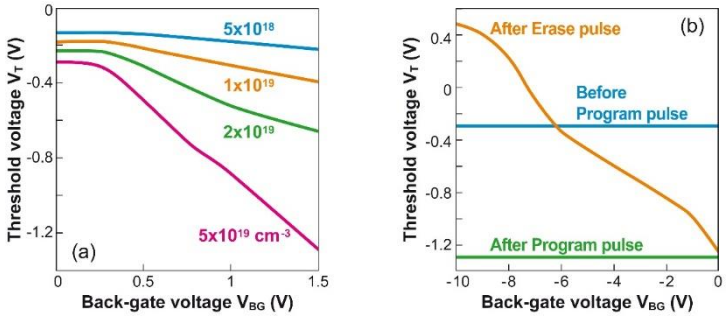

Fig. 2. (a) Threshold voltage lowering versus pulse amplitude. (b) Recovery of the initial V_T after a negative erase pulse.

In Figure 3, the gate length is scaled from 100 nm down to 18 nm. The beneficial effect of polarization is persistent and, interestingly, becomes stronger in very short transistors. In order to minimize the trap density, we have tested the option of capping the HZO layer with SiO_2. In such a composite Fe-BOX (SiO_2–HZO–SiO_2), the polarization effect remains substantial provided the cap is not too thick.

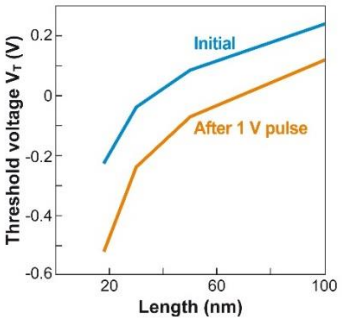

Fig. 3. Threshold voltage before and after programing versus gate length. The program pulse (1 V) and the ground-plane doping (N_D = 2x10^{19} cm^{-3}) are lower than in Fig. 2.

In summary, the replacement of a regular ‘passive’ BOX with an ‘active’ ferroelectric oxide is a tremendous opportunity for enhancing what is unique in FD-SOI devices, that is the dynamic control of the threshold voltage. Preliminary results confirm our concept and demonstrate that polarization effect increases the coupling rate by one order of magnitude. In addition, polarization-assisted back-biasing is a non-volatile mechanism, meaning that there is no need to maintain a constant back-gate voltage, one short pulse is sufficient. Since polarization switch is very fast (< 1 ns), the principle of Fe-BOX is applicable to RF circuits.

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Experimental Extraction of Self-Heating in SOI Nanowire MOSFETs at Cryogenic Temperatures

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The self-heating effect (SHE) is a notorious challenge when it comes to CMOS performance, particularly in the context of Silicon-On-Insulator (SOI) MOSFETs [1]. This phenomenon consists of the temperature increase in the conduction channel due to the heat flow generated by the drain current in addition to the difficulty of dissipating that heat, which is related to the high thermal resistance of the buried oxide of SOI devices. Furthermore, it is known that SHE is intensified in cryogenic environments [2], which is of major importance for specific applications such as quantum computing [3]. This work aims to demonstrate the experimental results of SHE in fully depleted (FD) Ω-gate SOI Nanowire MOSFETs obtained using the gate resistance thermometry technique in a wide temperature range from 300K down to 4.2K.

Fig. 1 presents a 3D schematic of an SOI nanowire with the two-contact gate structure, necessary for the self-heating extraction technique. The devices were fabricated at CEA-Leti following the process of [4]. Fig. 2 shows the measured drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for nanowires with L of 100nm and 40nm for ambient temperatures (T_{AMB}) from 300K down to 4.2K. The Zero Temperature Coefficient (ZTC) points demonstrate negligible series resistance in the whole temperature range. Fig. 3 presents the calibration of the electrical resistance of the metal gate (R_{GATE}), measured between the contacts Gate 1 and Gate 2, as a function of the ambient temperature (T_{AMB}) with the device in off-state. For the nanowire with L=100nm, in the linear region R_{GATE} increases with T_{AMB} at a rate of 0.37 Ω/K, while for L=40nm, the rate is 0.21 Ω/K. The variation of R_{GATE} with T_{AMB} is considerably smaller than that reported for planar FDSOI transistors in [5], which have a rate of 2.12 Ω/K. A saturation of R_{GATE} is observed for T below 20K, also demonstrated in [5]. Using the calibration curves from Fig. 3 and the I_{DS}-V_{GS} curves from Fig. 2, it was possible to extract the channel temperature increase (ΔT) as a function of the dissipated power ($P=V_{DS} \times I_{DS}$), with the results presented in Fig. 4. The increase of ΔT with the reduction of T_{AMB} demonstrates the stronger self-heating at lower temperatures. For $T_{AMB} \geq 50K$, the ΔT curves are roughly linear in the whole range of P. In contrast, below this temperature, the temperature increase presents a non-linear dependency with the power, where a steeper raise of ΔT is observed at the low power region, below 5μW. Fig. 5 compares the temperature increase between both channel lengths (100nm and 40nm) at same ambient temperatures, of 100K and 300K, indicating a higher ΔT for shorter devices: for a fixed power of 35μW, at T_{AMB}=100K the temperature increase is approximately 17K for L=40nm, while the nanowire with L=100nm heats up around 11K. Fig. 6 presents the differential thermal resistance (R_{TH}*), calculated as the derivative of the ΔT *vs.* P curves, as a function of the device temperature ($T_{DEV}=T_{AMB}+\Delta T$). The thermal resistance sharply increases below 70K, while a weaker dependency with the temperature is observed at higher T_{DEV}. This tendency agrees with the results of [6] for planar FDSOI transistors, although the R_{TH}* values are significantly higher for the nanowires, due to the thicker buried oxide layer (145nm, against 25nm of the planar device) and the highly confined active silicon region, both which hinder the heat diffusion.

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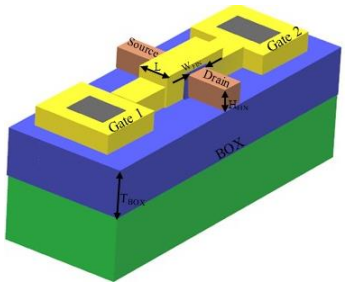

Figure 1 – 3D schematic of a nanowire with the 2-contact gate structure indicating the main geometrical parameters.

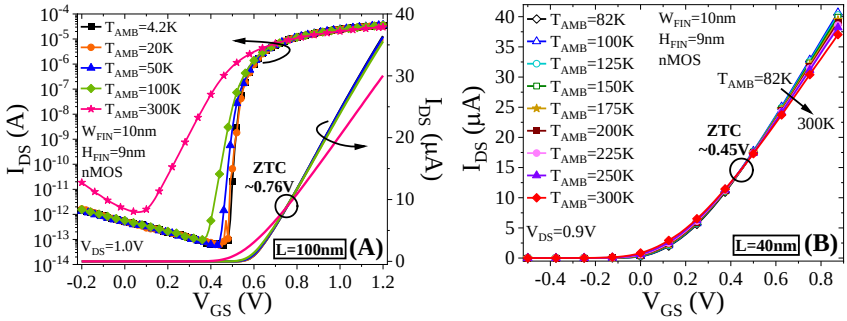

Figure 2 – Measured drain current as a function of the gate voltage for nanowires with (A) L=100nm and (B) L=40nm, both with W_{FIN}=10nm and H_{FIN}=10nm, at different ambient temperatures.

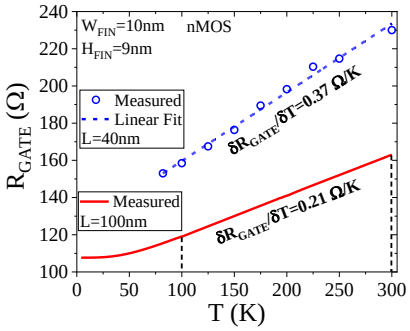

Figure 3 – Gate resistance as a function of the temperature for nanowires with L of 100nm and 40nm in off-state.

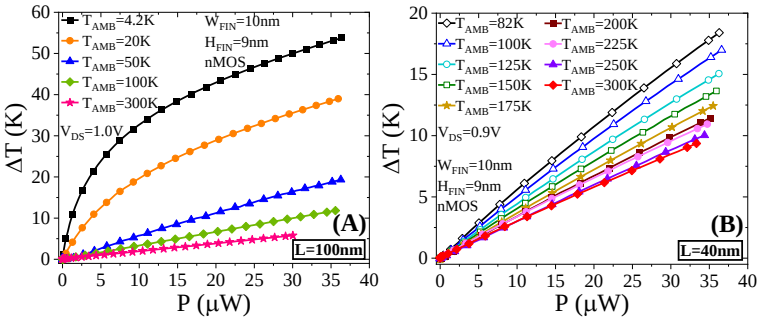

Figure 4 – Channel temperature increase as a function of the dissipated power for nanowires with (A) L=100nm and (B) L=40nm at different ambient temperatures.

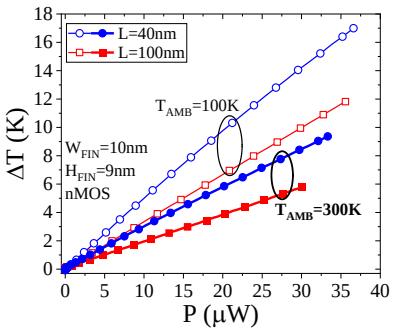

Figure 5 – Comparison of the channel temperature increase for nanowires with L of 100nm and 40nm at T_{AMB} of 100K and 300K.

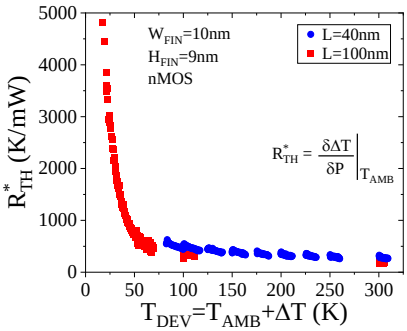

Figure 6 – Differential thermal Resistance as a function of the device temperature for nanowires with L of 100nm and 40nm.

Low-Loss Silicon Substrates with PN Passivation in 28 nm FD-SOI

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In RFICs signals propagate in metals atop insulator-semiconductor stacks, such as in a coplanar waveguide (CPW) is depicted in Fig. 1a. To avoid losses in such lines and coupling between them, the underlying substrate should present high *effective resistivity*. This is achievable using high-resistivity (HR) handle silicon, but beyond that, special passivation must be made at the Si/dielectric interface to avoid the formation of a highly conductive layer (inversion or accumulation). Such *parasitic surface conduction* can be countered using an interface rich in traps, though such solutions are incompatible with FD-SOI. This paper presents an alternative solution using PN junctions [1,2] applied to STMicroelectronics' 28 nm FD-SOI, run on HR substrates for the first time.

The principle behind the PN passivation is to interrupt the interface conduction layer with highly resistive depletion regions that are induced at alternating PN boundaries [1]. Fig. 2 plots the resistivity profile along the Si interface, highlighting the high-resistivity peaks at the PN junctions that dominate the value of the effective interface sheet resistivity. That sheet resistivity is higher-valued the larger the PN junction density per unit of distance along the interface. A depletion density can be defined as the ratio of W_{dep} over the pitch P (see Fig. 2). To maximize the depletion density, large values of W_{dep} and low values of P are sought [1,3]. W_{dep} is set by implant conditions, and lower-ranged doses are then preferred to maximize it [1]. Low values of P are achieved using the tightest lithography available in the process for substrate implants. However, using the most aggressive pitch can lead to undesired electrical coupling and connections between different wells. This problem is highlighted in Fig. 1c: if the depths of the N and P implants are not well balanced, using a tight-pitch results in connection between the deeper polarity wells via the region below the shallower wells. Fig. 1d shows that even if that same depth-imbalance exists while using larger pitch values, the problem is avoided.

Aiming for the best possible results using the tightest pitch values, 10 different wafers were processed with variations in the implant conditions attempting to achieve an optimal depth-implant balance suitable for the most aggressive pitch parameter. Fig. 3 plots the effective resistivity and line losses extracted [4] from the measured CPW lines (cross section and dimensions given in Fig. 3b for two types of CPWs) for select wafers. The results demonstrate for the M1LB lines that the 30 GHz losses can be reduced from 2.75 to 1.06 dB/mm using a high resistivity (around 1 kΩcm) substrate over the standard 10 Ωcm one, and that the loss can be further reduced down to 0.36 dB/mm when using the PN passivation (W09). Similar observations can be made for the IBLB lines (see Fig. 3c).

Table I and Table II recap the extracted effective resistivity and line loss values on all 10 wafer splits for the M1LB lines. Samples from Table I employ normalized P and N implant doses of 100%, while samples in Table II employ halved doses. The splits are made in N and P implant energies, to try and achieve ideal depth balance between neighbouring wells. The implant parameters pertaining to wafers W01, W02, W08, W04, W05 and W10 are imbalanced, with the N wells being deeper than the P wells, and parasitic N-well to N-well coupling happening in those wafers, bypassing the resistive depletion region at the interface, as depicted in Fig. 1c. Thanks to the split wafer processes, wafers W03, W07, W06 and W09 achieve good balance and high performance RF results by implanting the N wells shallower with reduced energy or by implanting the P wells deeper with higher energy. In those cases, effective resistivities up to 540 Ωcm can be achieved, with losses reduced to 0.36 dB/mm.

Experiments on the same 10 wafers utilising relaxed-pitch PN implant patterns below the same lines were run. When the PN pitch is relaxed to 2x the minimum value, all wafers achieve ρ_{eff} values in the range of 250 to 350 Ωcm. Since the depletion density is reduced (see Fig. 2), values of 400 to 540 Ωcm are no longer attainable, but the passivation becomes more robust to the implant conditions, since with that relaxed pitch, all 10 different implant parameters yield decent (~300 Ωcm) results.

Overall, this work demonstrates excellent RF substrate loss reductions in 28 nm FD-SOI.

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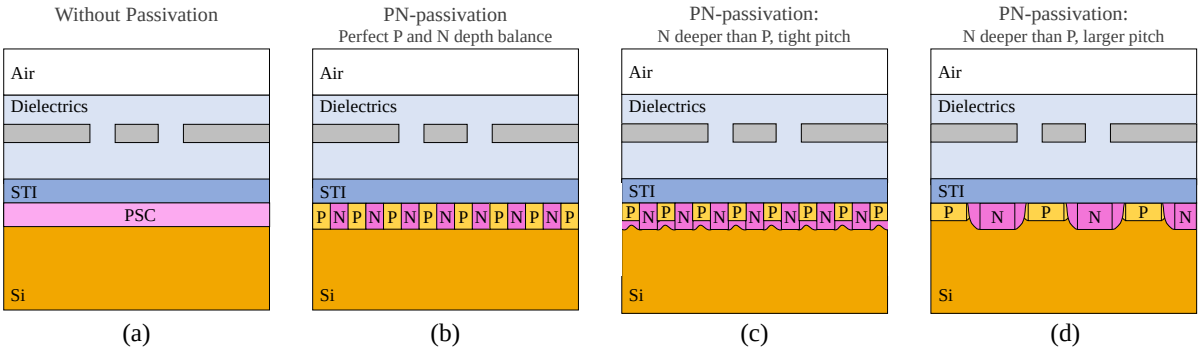

Fig. 1: CPW above (a) an unpassivated substrate with PSC (a), and above three types of PN-passivated substrates (b), (c) and (d).

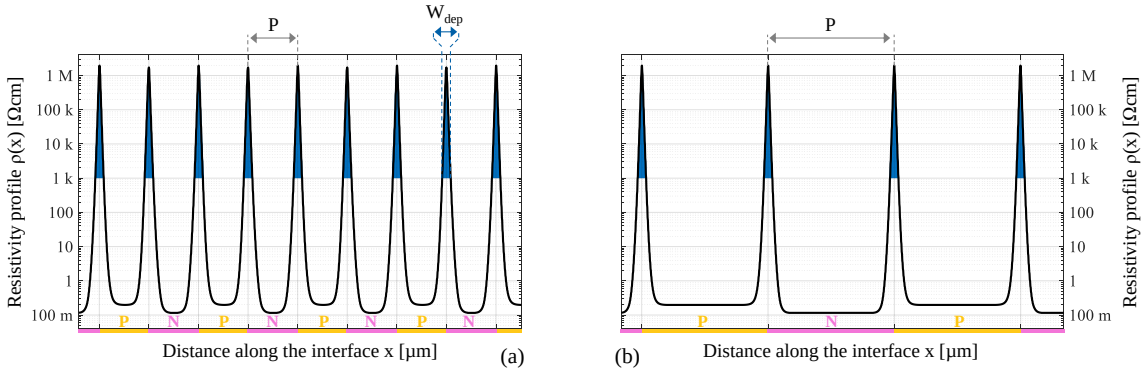

Fig. 2: Local resistivity profile ρ(x) along the Si/STI interface passivated with alternating PN junctions (obtained from TCAD simulations prior to wafer processing). (a) using a tight pitch achieving a depletion ratio of W_{dep}/P = 20%, and (b) using a relaxed pitch achieving 7%.

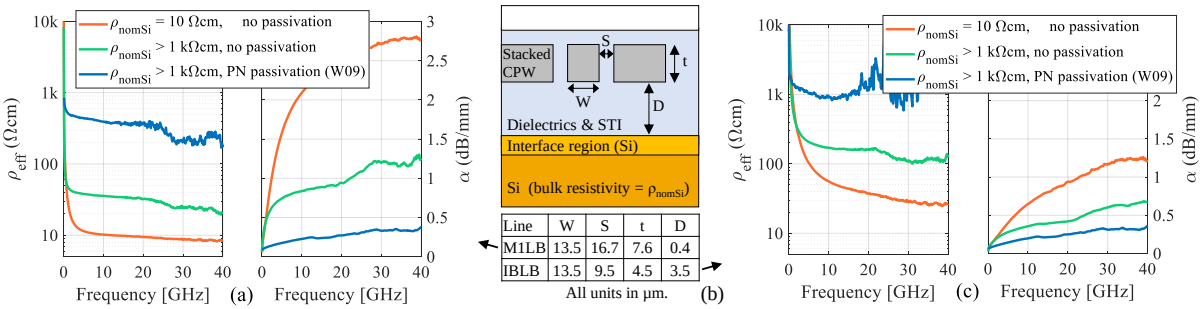

Fig. 3: Effective resistivity and line loss extracted from M1LB (a) and IBLB (c) lines for selected wafers. (b) Geometry of the CPW lines.

Wafer ID	Energy P [%]	Energy N [%]	ρeff [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W01	100	100	76	0.67	N too deep relative to P
W02	90	100	45	0.94	N too deep relative to P
W03	**110**	100	400	0.41	Good balance with **deeper P**
W07	100	**90**	400	0.42	Good balance with **shallower N**
W08	100	110	25	1.26	N too deep relative to P

Table I: RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 100%.

Wafer ID	Energy P [%]	Energy N [%]	ρeff [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W04	100	100	200	0.44	N too deep relative to P
W05	90	100	150	0.50	N too deep relative to P
W06	**110**	100	500	0.37	Good balance with **deeper P**
W09	100	**90**	540	0.36	Good balance with **shallower N**
W10	100	110	61	0.72	N too deep relative to P

Table II: RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 50%.

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[4] L. Nyssens *et al.*, *Internat. Jour. of Microw. and Wireless Techn.*, vol. 12, no. 7, pp. 615-628, June 2020.

Comparison of Self Heating Effect between SOI and SOSiC MOSFETs

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The requirements for electronic devices to withstand high temperatures have expanded, especially in sectors like oil exploration, aeronautics and automotive. Silicon-On-Insulator (SOI) MOSFETs are preferred for their fast switching and low leakage, showing superior high-temperature stability. However, they face self heating effect (SHE) due to poor heat dissipation through the buried oxide (BOX) [1]. SiC, with excellent thermal conductivity, is a better alternative to replace the BOX [2]. Using Si-on-SiC (SOSiC) substrates greatly improves the heat dissipation, reducing performance degradation due to SHE [3].

In this paper, we fabricated prototype SOSiC wafers by hydrophobic surface activation bonding (SAB) and analyzed the SHE of SOI and SOSiC MOSFETs using the calibrated TCAD simulations (Fig. 1). Their electrothermal properties, temperature rise, and thermal resistance are addressed. Furthermore, we investigated the heat dissipation paths of SOI and SOSiC MOSFETs, and elucidated the impact of the geometrical configuration of the devices on the relationship between temperature rise, thermal resistance, and dissipation pathways.

Fig. 2 shows that SOI MOSFETs suffer more serious on-state current degradation than SOSiC. At room temperature, the hot-spots are 347 K for SOI and 310 K for SOSiC, located near the LDD boundary due to uneven heat distribution (Fig. 3). The temperature rise and thermal resistance of the SOI MOSFETs are 3.9 and 4.1 times higher than those of SOSiC MOSFETs, which are more efficient in reducing junction temperature at same power levels. The comparison of the heat flux ratios across thermal contacts shows that SOI MOSFETs primarily dissipate heat through the drain and source (33.7% and 32.9%), while the substrate is the main heat path for SOSiC (85.6%), see Fig. 4 and 5.

As the epilayer thickness increases from 0.1 μm to 0.3 μm, the temperature rises in SOI by 52.4% despite the thermal resistance decreases by 1.8% (Fig. 6), which indicates that the increased current in thicker layers has a greater effect on SHE than the reduction in thermal resistance. For SOSiC, the temperature rise also increases for thicker layers but is limited to 15 K (Fig. 6). Meanwhile, heat dissipation through the source, drain, gate, and substrate indicates a correlation between dissipation paths and epilayer thickness (Fig. 6).

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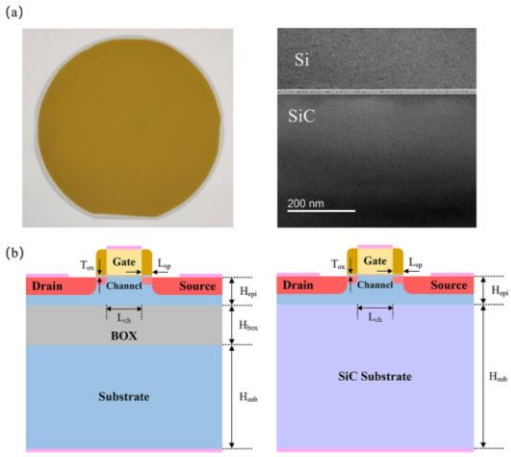

Fig. 1. (a) Photograph and TEM image of SOSiC wafer. (b) Structure of SOI and SOSiC MOSFET.

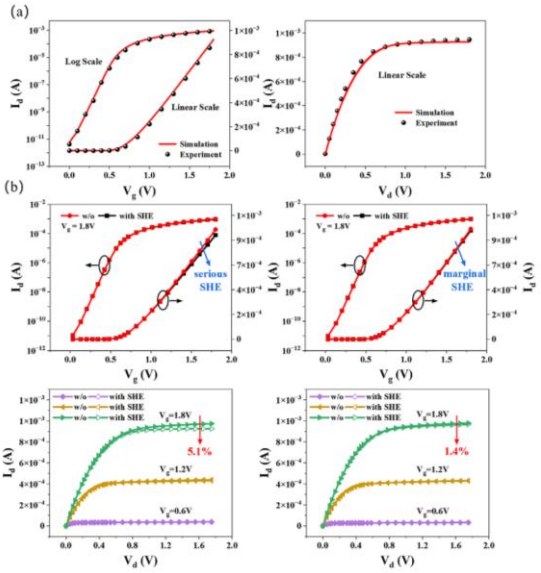

Fig. 2. (a) Calibration of SOI with experimental data. (b) The Transfer and output characteristic curves of SOI and SOSiC with and without the SHE considered.

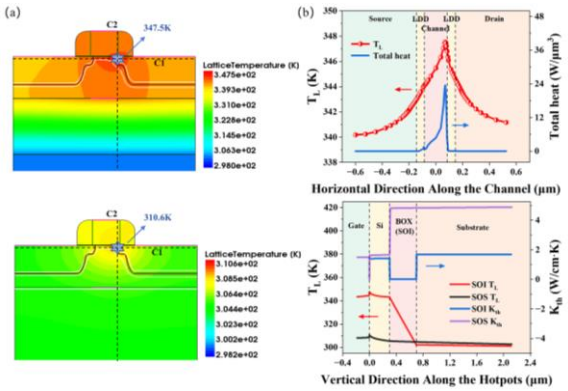

Fig. 3. (a) Lattice temperature distribution and the hotspot. (b) Temperature distribution in horizontal and vertical directions.

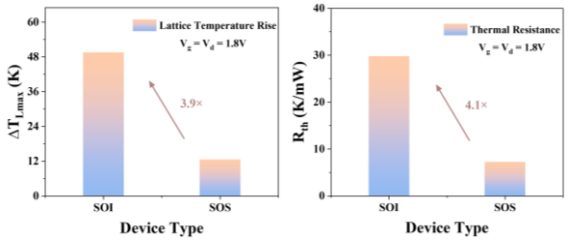

Fig. 4. Comparison of lattice temperature rise and thermal resistance between SOI and SOSiC.

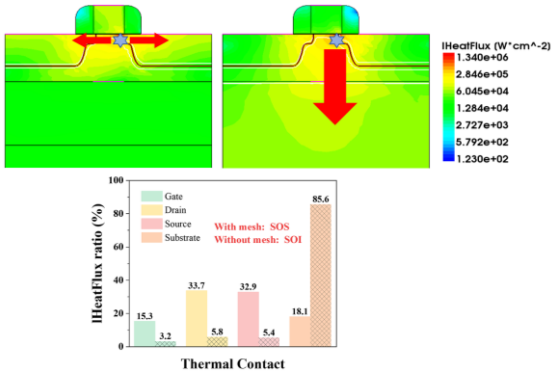

Fig. 5. Main heat dissipation paths and heat flux ratios across thermal contacts.

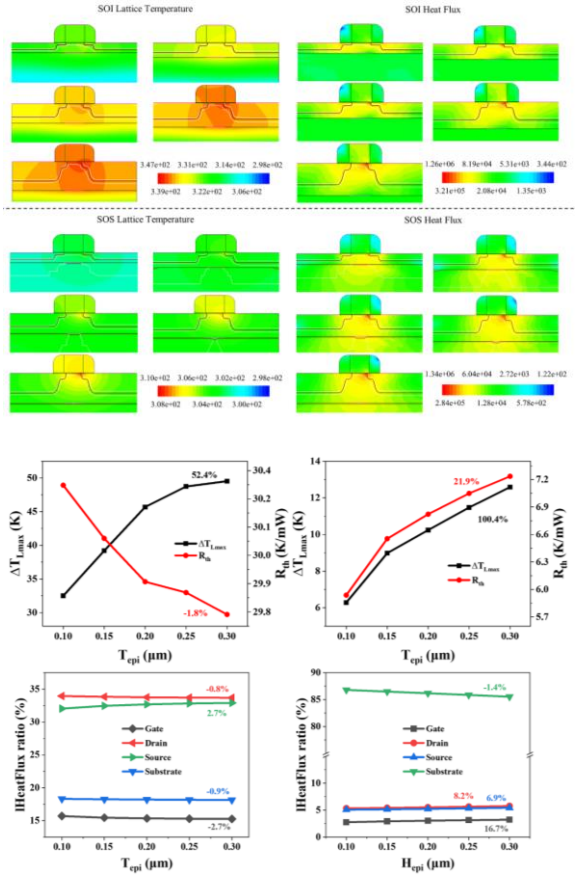

Fig. 6. Variation of the temperature rise, thermal resistance and heat flux width of SOI and SOSiC as H_{epi} increases from 0.1 μm to 0.3 μm.

Thermal-coupling characterization of FD-SOI FETs at cryogenic temperatures

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Quantum computers have the potential to solve problems computationally unfeasible on classical computers [1]. For proper operation, the qubits need to be cooled down to cryogenic temperatures with its control electronics placed in close vicinity. However, self-heating can raise the device temperature significantly above the ambient temperature and its surroundings [2,3], which degrades device performance and can also alter qubit state.

This work studies thermal cross-coupling between two side-by-side FD-SOI MOSFETs at liquid nitrogen temperatures in comparison to the room temperature one. We demonstrate that electrical parameters degradation caused by the operation (heating) of the neighbor device can be up to 50 % more important at 77K than at 295K.

Devices under study: The devices under study are fabricated by an industrial FD-SOI process. They consist of two multi-fingers nFETs placed side-by-side at 2.76 µm distance from each other (Fig. 1): (i) FET 1 features a gate length (L) < 30 nm and a total width (W) of 8 µm and (ii) FET 2 (heater) features L < 30 nm W of 32 µm.

Experimental results and discussion: Fig. 2 shows I_d-V_{gs} characteristics of FET 1 biased in a linear regime and different temperatures, highlighting a strong temperature dependence, particularly in the subthreshold region. The corresponding variations of g_m/I_d of FET 1 (Fig. 3) serve as a temperature calibration to estimate afterwards the temperature rise in FET 1 when FET 2 operates and its heat propagate to the surroundings. Fig. 4 plots I_d-V_{gs} curves of FET 1 biased in a linear regime when FET 2 is biased in cold FET mode ($V_2 = V_{gs2} = V_{ds2} = 0$ V) and in different operation conditions in saturation and strong inversion regimes (V_2 = 0.5, 0.6, 0.8 and 0.9 V) at both 77 K and 295 K. A linear reduction of g_m/I_d of FET 1 vs the power of FET 2 from 85.5 (31.1) to 74.6 (29.3) V^{-1} at 77 K (295 K) is highlighted in Fig. 5. By using g_m/I_d of FET 1 vs temperature plot (Fig. 3), one can estimate a temperature increase of ΔT = 46 K and 4 K at 77 and 295 K, respectively, demonstrating strong sensibility to thermal coupling (TC) effects at cryogenic temperature. Keeping this in mind, the following part of this work is focused on the analysis TC effect on various figures of merit (FoM) of FET 1, i.e. when it is operating in saturation regime. One of the main FoM for digital applications is the I_{on}/I_{off} ratio. While I_{off} is classically measured at $V_{gs} = 0$ V, I_d in this conditions becomes very small (< 10^{-10} A) at 77 K, so it is decided to take I_{off} at V_{gs} = 0.1 V in the framework of this work, so that $I_{on} = I_d(V_{gs} = V_{ds} = 0.8$ V) and $I_{off} = I_d(V_{gs} = 0.1$ V, $V_{ds} = 0.8$ V). As shown in Fig. 6, I_{on}/I_{off} ratio suffers a significant 77 % reduction at 77 K when FET 2 is biased at V_2 = 0.9 V while this reduction is limited to 25 % at 295 K. This degradation of the I_{on}/I_{off} ratio is strongly related to the increase of I_{off} (Table 1). Another FoM, particularly important for analog applications, is the transconductance (here extracted as peak value at V_{ds} = 800 mV), which appears only slightly degraded by the operation of FET 2 with a reduction of 1.7 % (1.5 %) at 77 K (295 K) (Table 1). Indeed, in saturation and inversion regimes FET 1 itself is subjected to self-heating making it less sensitive to external heat sources (e.g. cross-thermal coupling). In weak inversion regime (at V_{ds} = 800 mV) at $I_d = 10^{-7}$ A, g_m/I_d decreases with V_2 from 69.6 to 63 V^{-1} (-9.5 %) at 77 K and from 30.2 to 29.2 (-3.3 %) at 295 K (Table 1).

Conclusion: The impact of TC (and related temperature rise) was demonstrated on different FoM. Temperature rise in FET1 due to operation of FET 2 was revealed to be stronger at 77 K (ΔT = 46 K) wrt 295 K (ΔT = 4 K). FoMs degradation is more important at 77 K than 295 K with a maximum of 77% reduction of I_{on}/I_{off} at 77 K wrt 25 % at 295 K when the neighbor device is biased at 0.9 V due to stronger temperature increase at 77 K.

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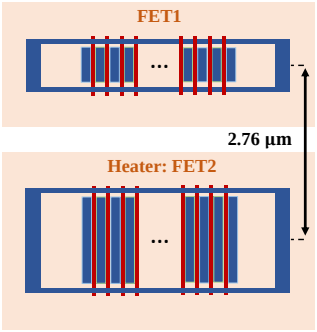

Fig. 1. Schematic (not to scale) of two multi-fingers FD-SOI nFETs placed 2.76 µm away from each other. Bottom FET is used to heat the top FET.

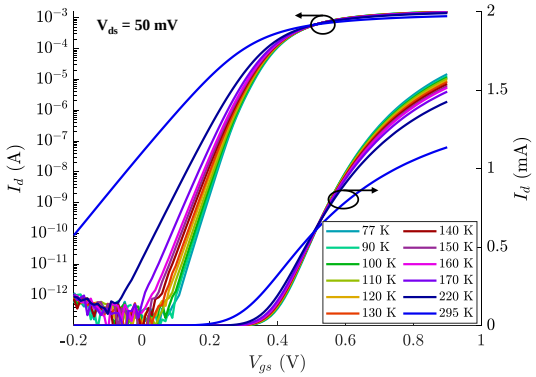

Fig. 2. Drain current I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at different temperatures.

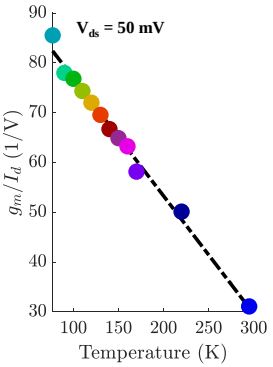

Fig. 3. g_m/I_d of FET 1 extracted at $I_d = 10^{-9}$ A vs temperature in linear regime (V_{ds} = 50 mV).

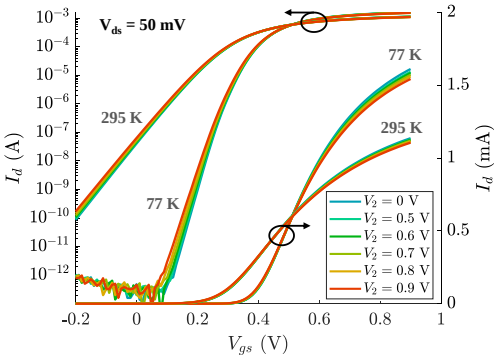

Fig. 4. I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at 77 K and 295 K when FET 2 is under different bias conditions.

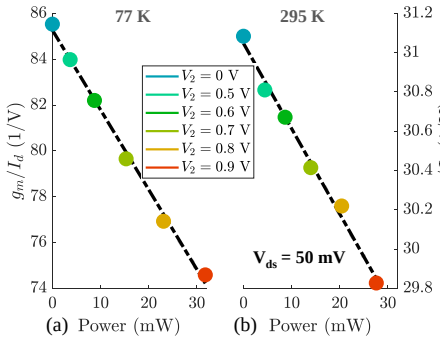

Fig. 5. g_m/I_d of FET 1 vs dissipated power of FET 2 at 77 K and 295 K, when FET 1 is biased at V_{ds} = 50 mV.

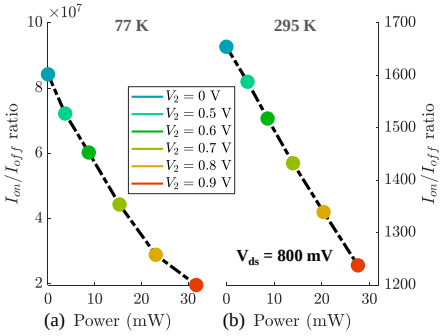

Fig. 6. I_{on}/I_{off} ratio of FET 1 vs dissipated power of FET 2 at 77 and 295 K, when FET 1 is biased at V_{ds} = 800 mV. I_{on} and I_{off} are respectively defined at V_{gs} of 0.8 and 0.1 V).

TABLE I. THERMAL-COUPLING IMPACT ON DIFFERENT FOM IN LINEAR (GREEN) AND SATURATION (BLUE) REGIMES.

FoM	Temperature (K)	V_2 = 0 V	V_2 = 0.9 V	FoM(V_2 = 0.9 V) vs FoM(V_2 = 0 V)
SS (mV/dec)	77	26.9	30.9	+ 14.9 %
	295	74.1	77.2	+ 4.2 %
V_{th} (V)	77	0.392	0.387	ΔV_{th} = - 0.005 V
	295	0.296	0.288	ΔV_{th} = - 0.008 V
I_{off} (A)	77	0.85×10^{-10}	3.60×10^{-10}	+ 323 %
	295	3.79×10^{-6}	5.03×10^{-6}	+ 32.7 %
I_{on}/I_{off}	77	84.2×10^{6}	19.6×10^{6}	- 76.7 %
	295	1.65×10^{3}	1.24×10^{3}	- 24.8 %
g_m (mS)	77	17.87	17.56	- 1.7 %
	295	13.58	13.37	- 1.5 %
g_m/I_d (1/V) @ $I_d = 10^{-7}$ A	77	69.6	63.0	- 9.5 %
	295	30.2	29.2	- 3.3 %

Enhancing Cryogenic Performance of FDSOI Logic Circuits Using Back Biasing and Threshold Voltage Engineering

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Introduction: The demand for low temperature circuits in various applications, including space electronics, data center power reduction, and quantum computing, necessitates the re-design and verification of the Room Temperature (RT) circuits designed for operation at cryogenic temperatures. Threshold voltage (Vth) increase with the temperature reduction is a major challenge, which can significantly affect circuit operation. This paper investigates the impact of back biasing and threshold voltage engineering on the performance of FDSOI based circuits at cryogenic temperatures. Additionally, we explore supply voltage (V_{DD}) reduction for power budgets and propose Vth engineering as a solution to optimize power/speed trade-offs.

Methodology: Predictive cryogenic spice compact models are developed for 22nm FDX technology using re-centering [1] of RT Process Design Kit (PDK) based on experimental measurement data and TCAD simulations across process corners and statistical variations to simulate the most likely behavior of circuit performance at low temperatures [2]. The re-centering procedure is necessary as the PDKs from the foundries are tailored for room temperature usage, and there are currently no available foundry PDKs designed specifically for cryogenic temperature applications. For the benchmarking of the circuit performance, we used a conventional 7-stage Ring Oscillator (RO).

Results and Discussion: The ring-oscillator circuit simulations are used to extract propagation delay and power dissipation per stage. The results obtained without using any back bias are summarized in Table 1. We observe reduced power per stage but increased propagation delay and reduced frequency at 4K compared to room temperature (300K). ***Impact of V_{DD} Reduction:*** Next, we reduce the supply voltage, and its impact on reducing the frequency and power dissipation is shown in Fig. 1 for the RO based on the TT corner devices for 300K and 4K cases with no back gate bias. Fig. 2 illustrates the higher Vth at 4K compared to 300K. The reduction in Vth when applying back bias is also demonstrated for 4K with the magnitude of back bias, $|V_{BG}|$ varying from 0 to 2V. ***Impact of Back Bias:*** We explore the impact of the back bias on the circuit performance, and the delay and power per stage as a function of V_{DD} and the results are shown in Fig. 3. ***Impact of Vth Engineering:*** We first reduce the Vth at 4K at zero back bias so as to match the off-state leakage at RT, and the results are shown in Fig. 4 including subsequent simulated characteristics at 4K with varying V_{BG}. RO simulation results are shown in Fig. 5, and we note that: (a) V_{DD} must be reduced at 4K to avoid increase in power dissipation, (b) maximum V_{BG} is always best for speed but may not be best when trading off speed vs power, and (c) the "sweet spot" is around V_{DD}=0.4V, V_{BG}=1V.

Conclusions: To achieve significant power reduction at cryogenic temperatures, a combination of back biasing and threshold voltage engineering is crucial. Back bias alone offers a maximum of 60% power reduction compared to RT, while the combined approach yields up to 4.5 times power reduction.

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Table1: RO simulation at RT and 4K.

	T=300K	T=4K
Delay/stage (pS)	2.74	2.93
Power/stage (µW)	11.40	10.47
Frequency (GHz)	26.18	24.30

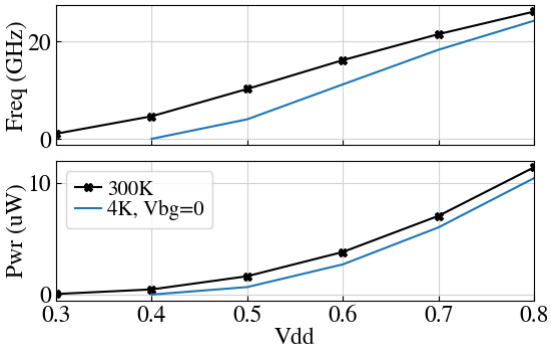

Fig. 1. Frequency and power per stage for V_{BG}=0V at TT corner.

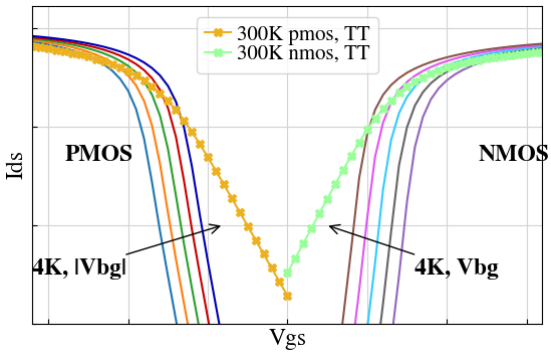

Fig. 2. I_D-V_G characteristics with back-gate voltage (V_{BG}) sweeps at 4K, and 300K results for reference (TT case).

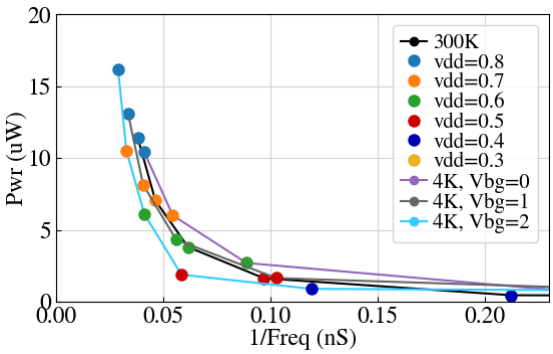

Fig. 3. Delay Vs Power dissipation for different V_{DD} and $|V_{BG}|$.

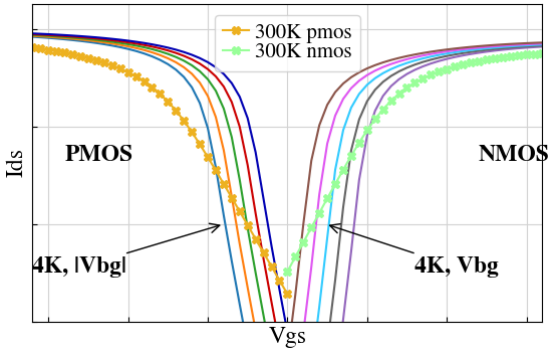

Fig. 4. Adjusted I_D-V_G at 4K to match Ioff at 300K, and subsequent impact of $|V_{BG}|$.

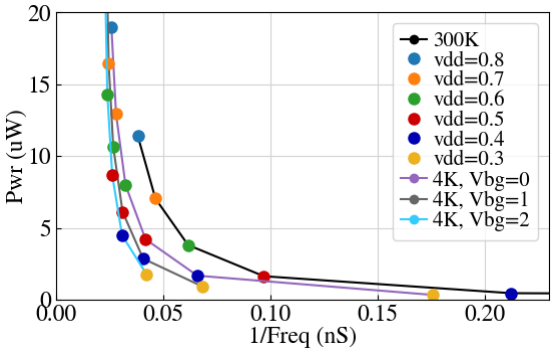

Fig. 5. Delay Vs Power dissipation for different V_{DD} using the Vth engineered devices under different $|V_{BG}|$.

High-Endurance Bulk CMOS One-Transistor Cryo-Memory

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Most proposed solid-state quantum sensing and computation schemes require cryogenic operation; any large-scale quantum circuitry will need integration with local CMOS-based control, storage, and data processing. We have previously reported on a compact bulk CMOS one-transistor (1T) memory that operates below 10 K via body charging due to impact ionization (II), with long retention times and very high ~10^7 I_1/I_0 memory window in quasistatic measurements [1]. Here we present the endurance and retention characteristics measured at 7 K in high-speed measurements.

Figure 1 summarizes the operating principle of the memory implemented in NMOS: at $V_D > 1.5$ V, as V_G is swept above V_T, II at the drain creates holes that charge the body to V_B and cannot leave without a low-impedance path to ground. These charges cause a threshold shift, creating positive feedback that switches I_D to a high value. Sweeping V_G back to zero traces out a loop, see Fig. 1(b), with a high ~10^7 ratio between I_1 and I_0 at $V_G = 0.3$ V. The retention time τ, extracted from the decay of V_B in Fig. 1(c), exceeds 10 minutes at 3 K in quasistatic measurements.

To test the endurance, speed, and retention time, the device was characterized at $T \sim 7$ K with fast time-domain measurements [2] in a low-T probe station with 50 Ω terminated probes and ~10 ns rise-time voltage pulses, as shown in Fig. 2, together with the write/sense pulse sequence. The fast measurement noise floor was ~0.15 μA, reducing the memory window compared to Fig. 1(b). Even so, a 100 cycle test program yielded a memory window of >1000 X above the noise floor, as shown in Fig. 3(a). Figure 3(b) shows long-term endurance: continuous write '1'/write '0' cycles were applied for 10^3–10^9 cycles, interspersed with the same 100-cycle memory test program. Setting the memory window at 250 X the noise floor, we find the device does not appreciably degrade over 10^9 cycles.

Figure 4 shows the retention time extracted from I_1 current sensing measurements as a function of hold time after write '1' (the '0' state has an uncharged body and is inherently stable, so I_0 is due to the noise floor). If the required I_1/I_0 window is set at 250 X, the retention time $\tau > 1$ s, whereas at 30 X $\tau >$ 10 s. These retention times are long on the quantum sensing or computation time scale (a comparable FD-SOI 1T memory using GIDL body charging [3] used a memory window of 2 X). However, they are shorter than $\tau \sim 800$ s obtained in the quasistatic measurement of Fig. 1(c) that used a >10^{14} Ω input impedance electrometer to measure V_B. This difference is due to substrate leakage during measurements as confirmed in Fig. 5, where τ extracted with an added 10 or 100 GΩ input resistor is ~10 s and 56 s. In a 1T memory with no substrate contact we thus expect $\tau \sim 800$ s, essentially nonvolatile.

[1] A. Zaslavsky, C. A. Richter, P. R. Shrestha, B. D. Hoskins, S. T. Le, A. Madhavan, and J. J. McClelland, *Appl. Phys. Lett.* 119 (2021) 043501.

[2] P. R. Shrestha, A. Zaslavsky, V. O. Jimenez, J. P. Campbell, and C. A. Richter, submitted to *J. Electron Dev. Soc.* (2024).

[3] W. Chakraborty, R. Saligram, A. Gupta *et al*., "Pseudo-static 1T capacitorless DRAM using 22nm FDSOI for cryogenic cache memory," in *Intern. Electron Dev. Meeting (IEDM)* (2021) pp. 40.1.1-40.1.4.

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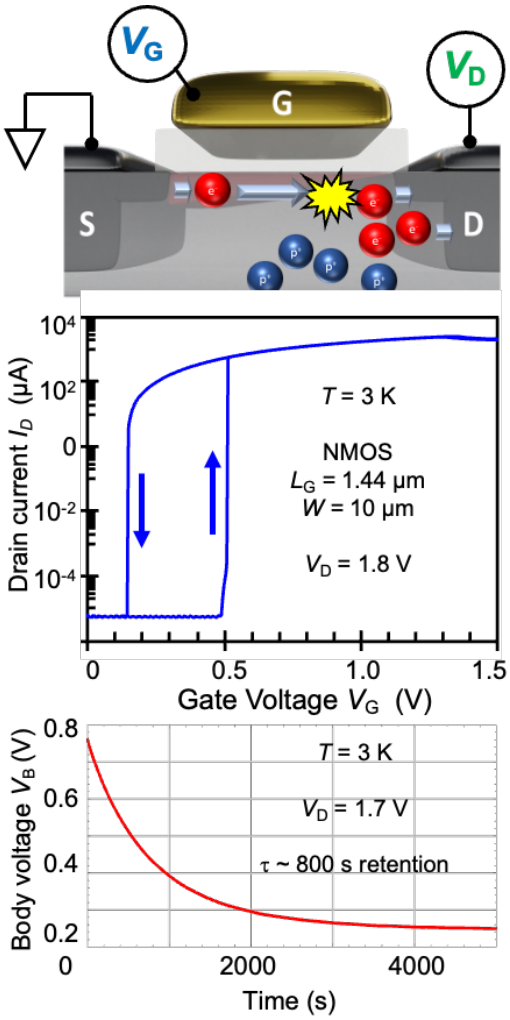

FIG. 1. (a) Schematic diagram of impact-ionization-induced charging of NMOS transistor body with holes for $V_D > 1.5$ V; (b) corresponding hysteretic loop in the $I_D(V_G)$ at $T = 3$ K and $V_D = 1.8$ V; (c) ~10 minute long decay of body potential V_B measured with a $>10^{14}$ Ω input impedance electrometer (adapted from [1]).

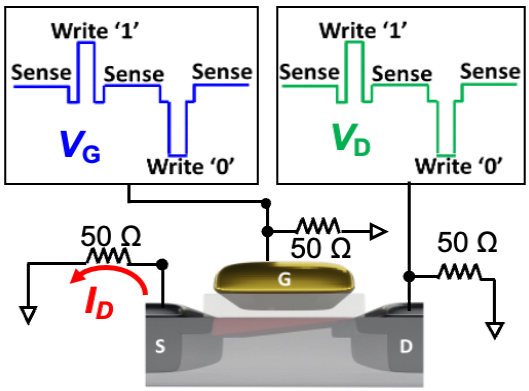

FIG. 2. Schematic high-speed measurement set-up in a cryostat at $T \sim 7$ K together with write '1' ($V_D = 2.1$, $V_G = 1$ V) // sense ($V_D = 1$, $V_G = 0.3$ V) // write 0' ($V_D = 1.5$, $V_G = -1$ V) // sense pulse sequence.

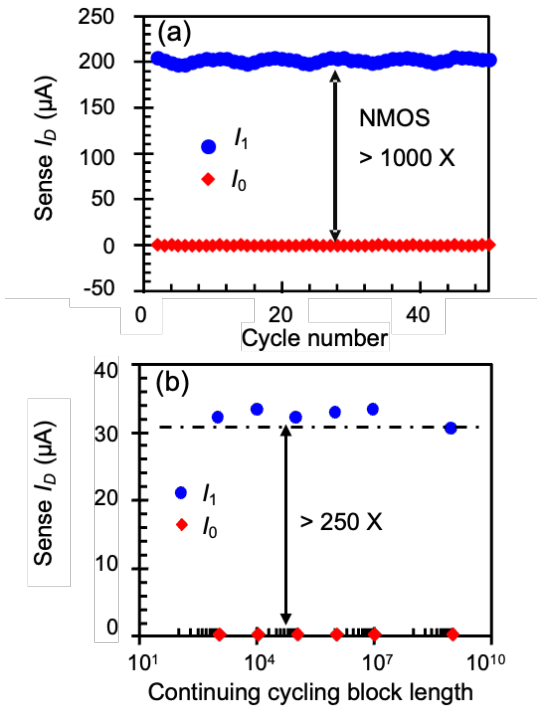

FIG. 3. (a) Raw cycling data for 1T NMOS cryo-memory at ~7 K ($L_G = 0.18$ μm, $W = 10$ μm), with I_1 sense current exceeding the ~0.15 μA I_0 noise floor by >1000 X; (b) long term endurance cycling with continuous multiple write '1'/write '0' cycle blocks ranging from 10^3 to 10^9 in order of magnitude steps followed by 100-cycle memory test program as in (a).

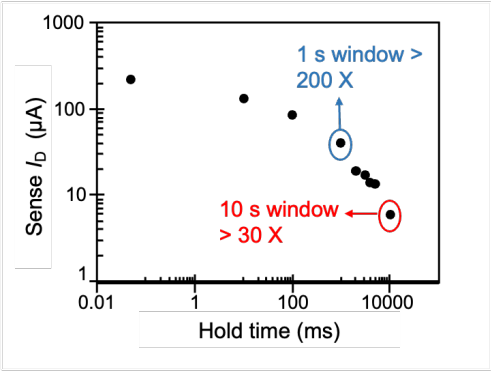

FIG. 4. Lower bound on retention time τ extracted from I_1 sense measurements after hold times of 100 μs to 10 s in order of magnitude steps.

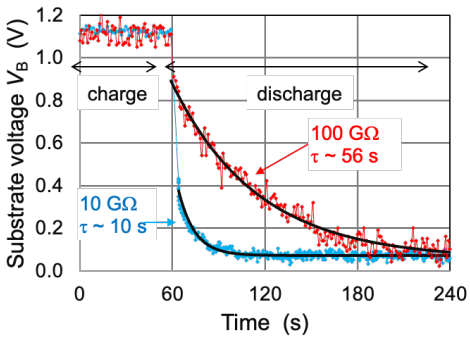

FIG. 5. Measured retention τ dependence on the input impedance of the measurement system.

Analysis of Electron Mobility in 7-Level Stacked Nanosheet GAA nMOSFETs

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Gate-all-around (GAA) nanosheet (NS) transistors have been proposed and demonstrated to be a competitive alternative to FinFETs, aiming to increase current drivability by footprint [1, 2], required to push the scaling limits of CMOS technology. The fabrication of GAA NS transistors with 7 stacked channels has been successfully presented, showing significant improvements compared to 2 levels [3]. It is well-known that in multiple-gate MOSFETs, current flows in different crystallographic planes, the orientation being (100) and (110) at the top/bottom and sidewalls, respectively, resulting in different mobility values. Therefore, this work details transport parameters of n-type 7-level stacked nanosheet GAA MOSFETs. The contributions of horizontal and sidewalls to mobility and degradation factors are analyzed separately in NS with several channel lengths.

The GAA Stacked NS nMOSFETs measured in this work were fabricated at CEA-Leti according to the process described in [3]. Fig. 1 shows a TEM and EDS spectroscopy of GAA NS transistors with 7 stacked channels [3]. The experimental mean drain current (I_D) as a function of gate voltage (V_G), and the transconductance (g_m) measured with a drain bias of V_{DS}= 25mV for NS with width W_{NS} = 15nm and 55 nm and different channel lengths (L) are presented in Fig. 2 and 3, respectively. The results clearly show that the subthreshold slope (SS) is close to the theoretical limit even for the device with L = 50 nm and W_{NS} = 55 nm, which presents SS = 60.5 mV/dec, showing excellent electrostatic control. Aiming to separate the contribution of horizontal (top and bottom channels) and vertical (sidewalls) conduction planes, the drain current has been plotted as a function of the nanosheet width for different values of V_G, with the sidewalls current ($I_{D,side}$) obtained at W_{NS} = 0 [4]. The current on the 13 horizontal conduction planes ($I_{D,top}$) is then calculated as the difference between I_D and $I_{D,side}$. The top and sidewalls components of I_D and g_m for the devices with L = 100 nm and different W_{NS} are presented in Fig. 4. As the NS is narrowed, approaching the silicon film height (H_{NS}), the contribution of the sidewalls in the total I_D becomes of the same order of magnitude than the horizontal planes. The threshold voltage (V_{TH}), low-field mobility (μ_0), and its degradation factors were extracted from these curves using the Y-Function methodology. As shown in Fig. 5, the V_{TH} of the sidewalls is slightly larger than at the top, which is responsible for fixing the overall V_{TH} of the devices, independent of L or W_{NS}. From the results shown in Fig. 6, one can note that, unlike observed for FinFETs, the sidewall mobility is not reduced compared to that in the horizontal conduction planes. The linear and quadratic mobility degradation factors, θ_1 and θ_2, are presented in Figs. 7 and 8, respectively. The extracted results for θ_1 (related to phonon and Coulomb scattering) and θ_2 (related to surface roughness), show that both degradation factors are larger at the horizontal surfaces than at the sidewalls regardless of L. Negligible θ_1 is observed at the sidewalls, which contributes to reducing the overall θ_1 in narrow NS. On the contrary, θ_2 has been shown to increase as the NS is narrowed.

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[4] K. Bennamane, et al., Solid-State Electronics, 53, p. 1263 (2009).

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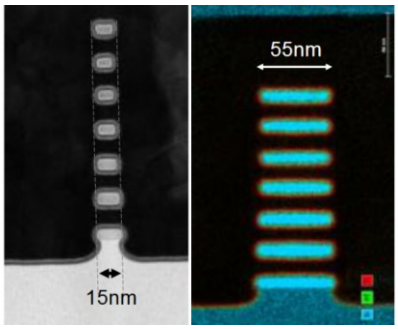

Fig. 1. TEM and EDS spectroscopy of GAA NS transistors with 7 stacked channels [3].

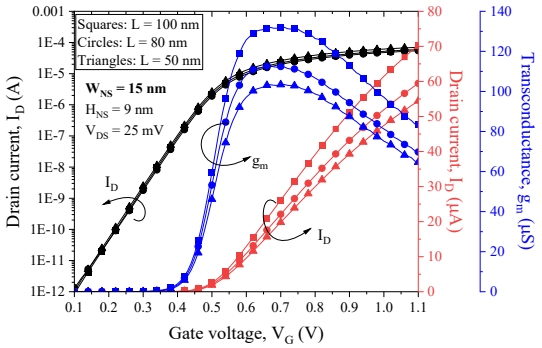

Fig. 2. Experimental mean drain current and transconductance as a function of the gate voltage, for GAA stacked NS with W_{NS} = 15 nm and different L.

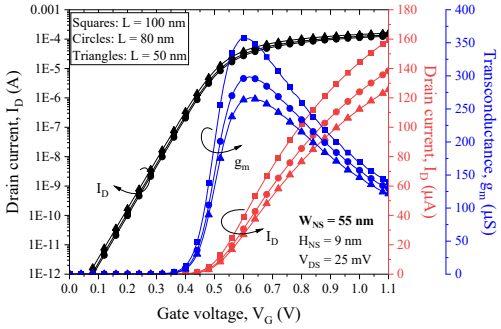

Fig. 3. Experimental mean drain current and transconductance as a function of the gate voltage, for GAA stacked NS with W_{NS} = 55 nm and different L.

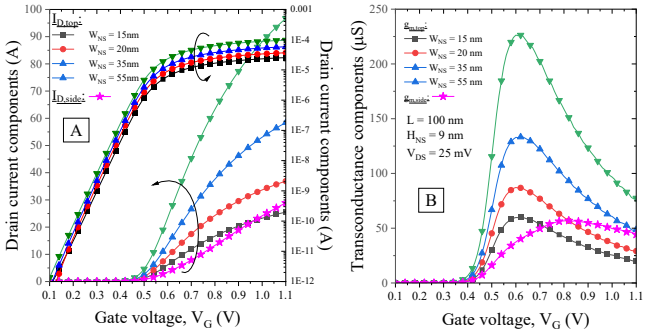

Fig. 4. Top/bottom and sidewalls components of I_D (A) and g_m (B) as a function of the gate voltage for stacked GAA NS transistors with L = 100 nm and different NS widths. All curves measured with V_{DS}= 25mV.

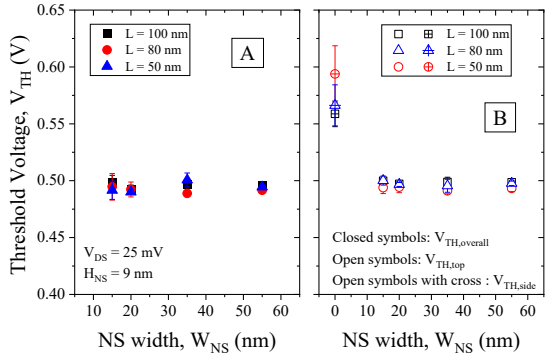

Fig. 5. Total, top and sidewall threshold voltage *vs* W_{NS} for GAA stacked NS with different channel lengths.

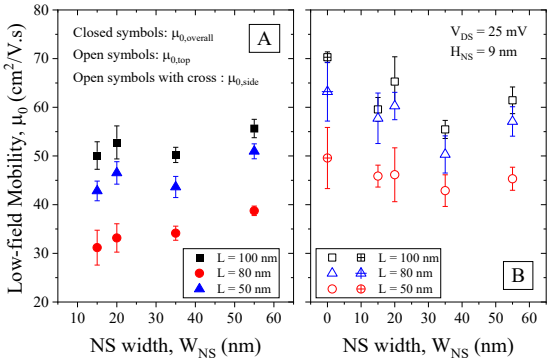

Fig. 6. Total, top and sidewall low-field mobility *vs* W_{NS} for GAA stacked NS with different lengths.

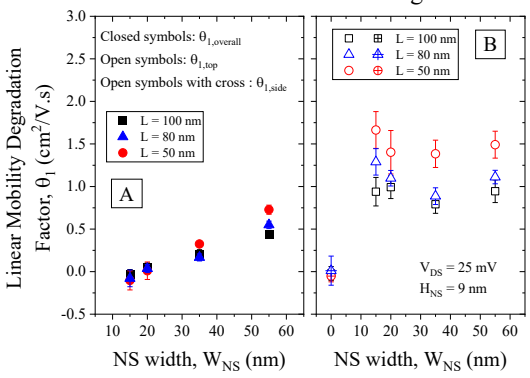

Fig. 7. Total, top and sidewall linear mobility degradation factor *vs* W_{NS} for GAA stacked NS with different channel lengths.

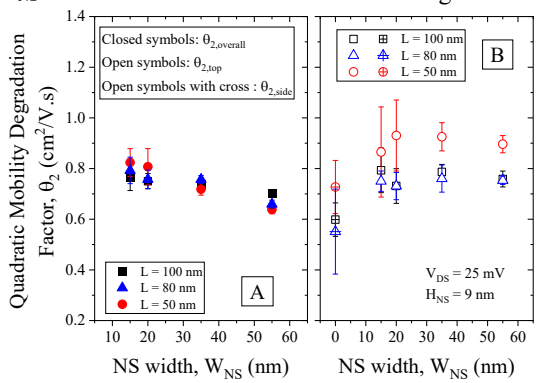

Fig. 8. Total, top and sidewall quadratic mobility degradation factor *vs* W_{NS} for GAA stacked NS with different channel lengths.

Mobility and intrinsic performance of silicon-based Nanosheet FETs at 3nm CMOS and beyond

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***Abstract*—Nanosheet Field-Effect Transistors (NSFETs) have been introduced in the 3nm CMOS technology due to advantages over the FinFET technology. In this paper, using our in-house NanoElectronics Simulation Software (NESS), we explore the mobility and the intrinsic performance of NSFETs for different channel orientations. The effective masses for different cross-sections and channel orientations are extracted from the first principal simulations. The mobility and the intrinsic performance will be evaluated using the effective mass based on the non-equilibrium Green's function (NEGF) and Kubo-Greenwood simulation engines of NESS. The proposed work provides insight into the optimised parameters for NSFET configurations suitable for 3nm and further technology nodes.**

***Keyword-component*—Nanosheet, field-effect transistors, NSFET, NEGF, QuantumATK, first principle, NESS**

I. Introduction

NSFETs have been already adopted in the 3nm CMOS technology and show potential for 2nm CMOS and beyond. The nanometer thickness of NSFET is more easily achievable if compared to FinFETs due to the planar orientation of the channel comparing to the vertical orientation in FinFETs [1]. However, the reduction of the NSFET thickness and cross section dimension changes the key physical parameters of the bulk values that require multi-subband transport in order to accurately capture the device performance.

The crystallographic orientation of channel material can significantly impact the electronic and transport properties of NSFETs [2], [3]. NSFETs with [100] channel orientation show excellent device performance, in comparison to [110] and [111] channel orientation. This is due to the symmetry of the crystal structure, which allows for better alignment of the atoms, leading to better charge transport and current. NSFETs with [110] orientation have higher electron mobility than those with [100] due to their anisotropic crystal structure. The [111] orientation is the least commonly used crystal orientation in NSFETs due to its high surface energy, which makes it difficult to growth. However, all of these NSFETs are gate-all-around architectures and anysurface defects on the channel can result in fluctuation of the leakage current and on/off ratios.

The cross-sectional size of NSFET is another key factor that also significantly impacts its performance [4]. As the cross-sectional size decreases, the transistor's dimensions approach the quantum confinement limits, which impacts the electronic properties of the channel material. A smaller cross-sectional size leads to a higher surface-to-volume ratio, which increases surface effects, and, as a result, decreases the mobility resulting in poor device electrical characteristics [5]. Therefore, understanding the effect of different cross-section sizes on the performance of NSFETs is crucial.

II. Results and Discussions

The cross-sections of devices simulated in this work are illustrated in Fig. 1(a). They represent the 3nm CMOS technology, with a channel cross-section of 3×12nm and 1nm oxide thickness surrounding it. In this study we consider only n-channel transistors although NESS has also a p-channel NEGF engine. The NESS Structure Generator (SG) can introduce the common sources of statistical variability. Here, we have applied Surface Roughness (SR) at the channel/oxide interface as shown in Fig. 1(b), which will be used when the effects of surface roughness and confinement fluctuation scattering are investigated.

Transport is carried out with the electron effective mass NEGF transport module of (NESS) [6]. The simulation flow starts with the first principle band structure simulations using QuantumATK for various cross-sections and channel orientations as shown in Fig. 1(c). The Effective Mass Extractor (EME) module included in NESS is used to extract the transport and confinement effective masses by using parabolic band approximation with the correct minima extracted from the sub-band dispersion relations. Accordingly, the effective masses for each orientation, for multiple cross-sections, from 3×3nm up to 3×12nm, are shown in table I.

In Fig. 2, we have shown that our parabolic approximation is in agreement with the minima of the conduction band for all three orientations and for both the 3×3nm and 3x12 nm cross-sections. Table II represents the deformation potentials and energies for intra- and inter-valley transitions within the optical scattering mechanism. Moreover, utilising the aforementioned values, in fig 3, we present the ballistic, e-ph (PH) and PH+SR scattering I_D-V_G characteristics of two types of device cross-section, i.e., strong confinement (3x3nm) and bulk-like masses (3x12nm). Based on our results we can conclude that for all devices the drive current (Ion) is higher for ballistic as compared to other scattering mechanisms. Also, there is a minimal difference in the leakage current (Ioff) for all orientations. Consistently with the physics and theory both Ion and Ioff current increase with the increment in the cross-section dimension with a slight decrement in Ion/Ioff ratio due to the loss of the electrostatic gate control. In summary, our work shows that NSFET with [110] crystal orientation and 3x3nm cross-section performs the best in comparison to [100] and [111] devices both at low and high drain bias. This is due to the variation in effective mass for the z-valley along the y-direction that increases the possible recombination with asymmetry between the y and z-directions.

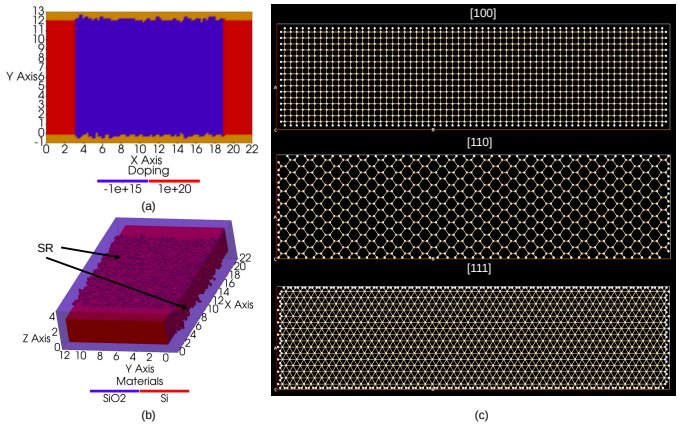

Fig. 1. (a) The SG 2D representation of the doping profile of the 3×12nm NS, cross-section of the z-axis along the channel. (b) The SG 3D representation of the 3×12nm NSFET section showing the Surface Roughness of the channel. (c) The crystalline cross-section from QATK for orientations [100] (top), [110] (middle), and [111] (bottom).

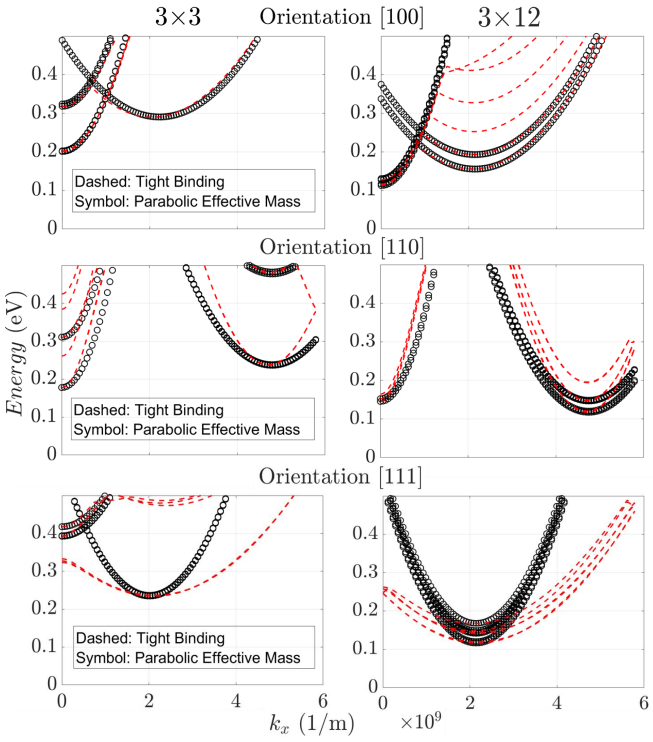

Fig. 2. Comparison of the low conduction band minima of the QATK TB and the Parabolic approximation from NESS for cross-sections 3×3nm and 3×12nm – orientations [100] (top), [110] (middle) and [111] (bottom).

TABLE I

Extracted effective masses from the EME module of NESS for orientations [100], [110], [111] across four different cross-sections with 3nm height.

		[100]			[110]			[111]		
Width [nm]	Valley	m_y [m_0]	m_z [m_0]	m_x [m_0]	m_y [m_0]	m_z [m_0]	m_x [m_0]	m_y [m_0]	m_z [m_0]	m_x [m_0]
3	Δ_x	0.278	0.278	0.945	0.496	0.259	0.568	0.763	0.22	0.455
	Δ_y	1.03	0.251	0.271	0.489	0.258	0.568	0.765	0.218	0.455
	Δ_z	0.251	0.993	0.271	0.303	0.908	0.164	0.229	0.661	0.455
6	Δ_x	0.239	0.273	0.935	0.257	0.374	0.509	0.316	0.371	0.428
	Δ_y	0.524	0.372	0.24	0.263	0.361	0.509	0.32	0.356	0.428
	Δ_z	0.544	0.36	0.24	0.955	0.28	0.159	0.417	0.28	0.428
9	Δ_x	0.478	0.281	0.954	0.587	0.375	0.526	1.116	0.383	0.426
	Δ_y	1.167	0.375	0.239	0.61	0.363	0.526	1.089	0.368	0.426
	Δ_z	1.274	0.36	0.239	2.303	0.284	0.169	1.189	0.307	0.426
12	Δ_x	0.206	0.281	0.959	0.265	0.377	0.518	0.279	0.378	0.427
	Δ_y	0.525	0.375	0.236	0.274	0.364	0.518	0.268	0.366	0.427
	Δ_z	0.592	0362	0.236	1.049	0.281	0.171	0.295	0.303	0.427

TABLE II

Deformation potentials and energies considered for different branches in the optical scattering mechanism. The D_P for acoustic phonon is set to 14.5eV.

Optical Phonon Type	D_P (eV/m)	Energy (eV)
g-type, TA	5×10^9	0.012
g-type, LA	8×10^9	0.0185
g-type, LO	11×10^{10}	0.063
f-type, TA	3×10^9	0.0189
f-type, LA	2×10^{10}	0.0474
f-type, TO	2×10^{10}	0.059

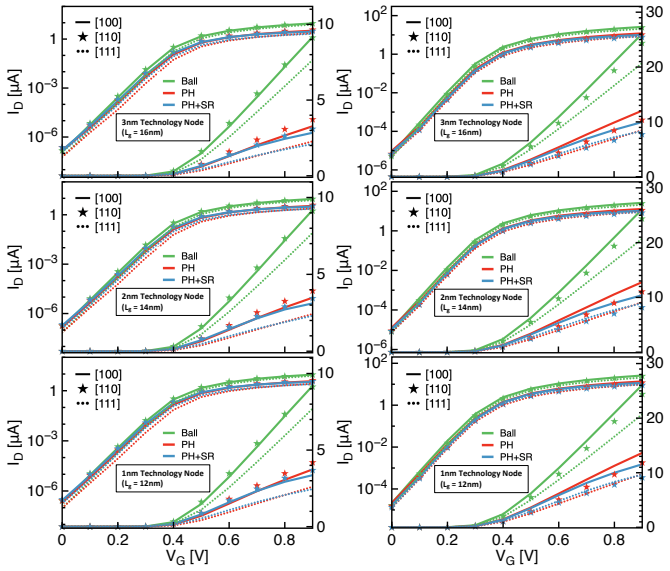

Fig. 3. 3nm and beyond (top to bottom) I_D-V_G characteristics at V_D = 0.05V for (left panel) 3×3nm and (right panel) 3×12nm cross-section. PH represents the combined optical and acoustic scattering processes. Δ_{rms} and correlation length for SR scattering are set to 0.4 and 1.3nm, respectively.

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Preliminary numerical study on magnet gate in MOS FD-SOI for quantum and sensor applications

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Abstract:
This preliminary study aims to report a possible new MOS device with a stack of magnetic gates, for example in 28 nm FD-SOI UTBB technology. This study focuses on a proposed stacking in a MOS gate through 3D HFSS numerical simulations to evaluate the magnetic field gradient under and around the MOS device. Typically, the polycrystalline gate is replaced by a magnetic material with metallic behavior to also enable conventional electrostatic MOS control. The dimensions meet 28nm design requirements and Co or Ni magnetic materials are candidates for process integration. In addition, other materials should be selected based on the magnetic specifications and metal work function. Applications could be with an internal or external magnetic field environment for quantum or sensor applications. 3D magnetic simulations are carried out with the HFSS tool.

Keywords- FD-SOI CMOS, cryogenic temperatures, 3D FEM simulation

I. INTRODUCTION

The purpose of this article is to report the main numerical results on a combo function at the MOS gate level in FD-SOI technology for quantum or sensor applications. One of the promising candidates is FD-SOI technology which today demonstrates relevant performances in low power consumption for RF/analog/digital design at cryogenic temperature. Therefore, 28nm ultra-thin body buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) technology is explored based on these typical dimensions, materials, and process steps. Figure 1 gives a cross-section view of a MOS device and shows the typical gate stacking process with a 2D MOS TCAD shape. From top to bottom, the stack consists of a silicide (CoSi2) contact on a polycrystalline silicon (p-Si) gate pillar, followed by a metal (TiN) gate compatible with the middle of the silicon band gap which is on a high k dielectric. This high k hafnium (HfO2) is the gate oxide (Tox). Afterwards, we find a thin silicon film (Si film) for the electronic channel which is placed on a buried oxide (Box) and which is on a bulk silicon substrate (Handle substrate). MOS electrostatic control is provided by the metal work function, by the top gate voltage and if necessary, by the additional back gate bias. For a qubit and for example, EDSR control requires a magnetic field gradient close to the qubit that could be integrated into the back end of the line (BEOL) with a Co micromagnet or other magnetic material. A 3D quantum TCAD simulation on an ideal topology result in a Rabi frequency of f_R = 4.7 MHz. However, the micromagnet is quite far from the area of interest and minimizes the impact of the magnetic field gradient. The main idea here is therefore to replace a part of the gate stack (silicide/poly/metal grid) with a magnetic material with metallic behavior and which complies with the work function for the MOS electrostatic control. Figure 2 shows a top view of a possible standalone qubit where the quantum dot is at the center of the device. Also reported is a 2D HFSS (z-axis) view of the device stack with a zoom in on the Co/Tin/HfO2 /Si/Box/Si structure as a first device proposal. Figure 3 gives the two types of devices studied where the metal gate is the TiN or Co material. In this case, a 100 mV offset of the metal work function is between these two metals. This voltage offset could be restored by biasing the back gate and maintaining the control of the initial front gate voltage. Figure 4 gives for structure #1 the vector mapping of the magnetic field and the magnitude mapping centered on the quantum dot in two conditions: for the vertical and horizontal orientation of the magnetic field of the micromagnet with 1T (au). Numerical simulation extractions in both cases show that the gradient is well below the gate MOS in the quantum dot and that the magnetic spreading is consistent with the dimensions of this device. The following figure 5 concerns structure #2 where the metal gate is a ferromagnetic material, here Co. We extract from the previous one that the magnitude is 4% higher than the previous case due to the shield of TiN. Thus, the two process solutions could be integrated without major change in device behavior (except reverse bias if necessary). Furthermore, for (accurate study of the magnetic gradient mapping in the entire device, several Z-cut planes are extracted and presented in Figure 6. In conclusion, a micromagnet embedded in the gate stack with suitable magnetic material and electrical conductivity is a future way to enable efficient electrostatic control of the MOS device as a quantum dot function and provide a magnetic gradient for the spin control via the EDSR technique. Additionally, the material hysteresis curve is an important feature for Hc and Hr values as a function of the external magnetic magnitude of the Zeeman effect required for spin manipulation.

ACKNOWLEDGMENTS

The authors of this article would like to thank all colleagues at STMicroelectronics and 3IT who contributed to these results within the standard 28 nmFD-SOI process. A special thanks to Michel Pioro-Ladriere for the fruitful discussion on this topic.

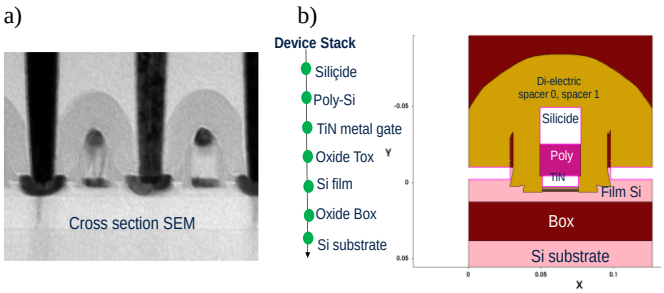

Figure 1: a) FD-SOI MOS cross section, b) TCAD MOS transistors with gate stack .

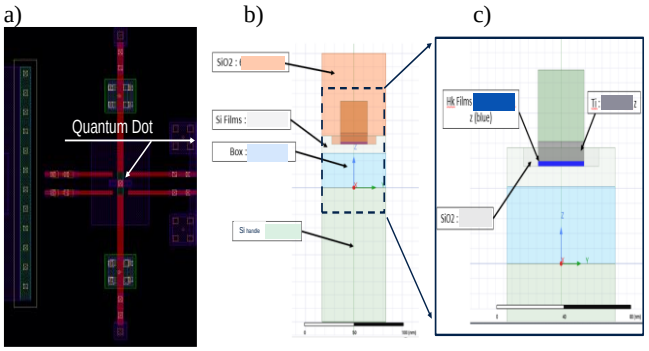

Figure 2: a) top view on a standalone Qubit Layout in 28FD-SOI b) 2D view in HFSS in z axe c) zoom in stack : Co/TiN/HfO2/Si/Box/Si

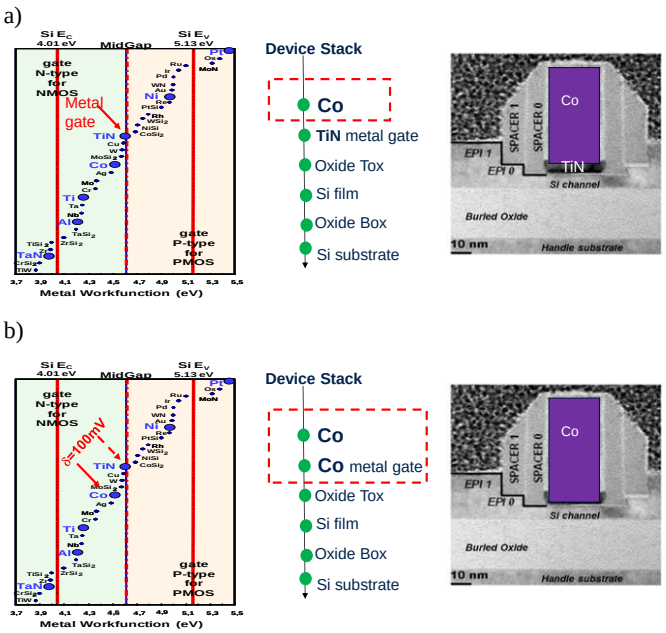

Figure 3: a) Stack structure #1 : Co/TiN metal gate b) stack structure #2 Co/Co metal gate (all other elements are kept identically)

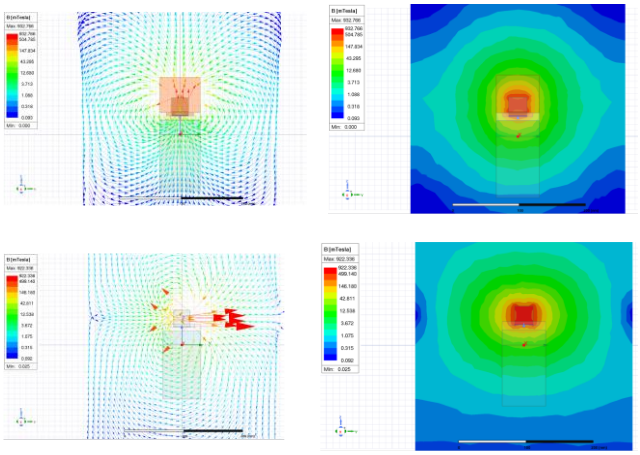

Figure 4: a) Vertical mapping of magnetic vector and magnitude b) Horizontal mapping of magnetic vector and magnitude (1T au)

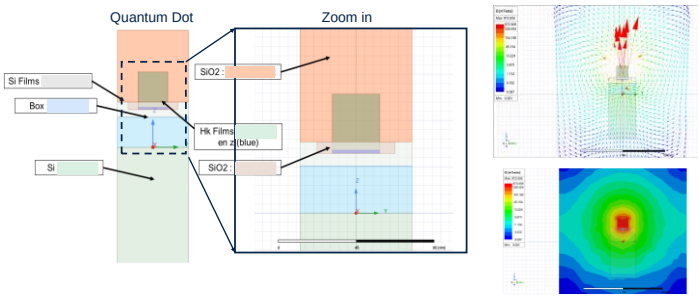

Figure 5: a) Stack structure #2 with Zoom in and with vector /magneitude map extractions

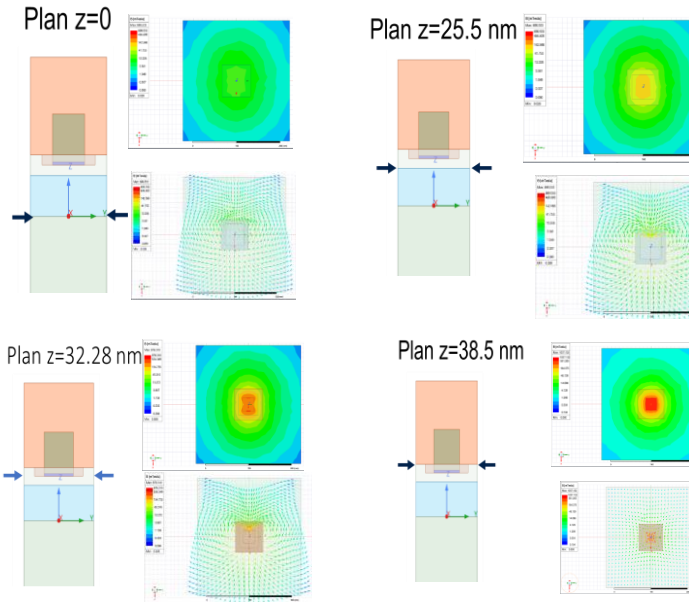

Figure 6: cut plan extractions for differente deepth z=0 ; 2,5 ; 32,28 & 38,5 nm

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Epitaxial p+pn+ vertical short diodes for microbolometers

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***Abstract*—In LWIR band, pn diodes represent an attractive solution for thermometers in microbolometers. In this paper, epitaxial short p^+pn^+ diodes were studied at 303-353 K. A TCC at 4.6-6.2 %/K and a noise dominated by ficker noise were measured. Finally, a thermal resolution between 2.10^{-3} *K* and 5.10^{-2} *K* was obtained at 303 K. It offers promising performances for future microbolometers.**

Keywords—pn-diode, silicon, thermal sensors, LWIR, TCC, flicker noise, thermal resolution, epitaxy

I. INTRODUCTION

The Long-Wave Infrared (LWIR) band, covering the wavelengths from 8 µm to 14 µm, is a region of the light spectrum used for thermal imaging sensors. It offers a high contrast in low visible light conditions and therefore interests in multiple applications : military, rescue, medical, spatial, automotive emergency breaking (AEB) for instance. In this wavelength range, uncooled thermal detectors as microbolometers are used. Their thermometers are usually made of a semiconductor resistance, commonly vanadium oxides (VO_x), amorphous silicon (a-Si) and titanium oxides (TiO_x). They feature a relative thermal response ranging from -1.5 to -3.3 %/K and a very low noise at low frequencies [1]. As an alternative to classic semiconductor resistances, forward biased silicon pn diodes offer several advantages : a compatibility with CMOS technological processes and a relative thermal response at 4-7 %/K for currents ranging from 1 nA to 1 µA. In addition to previous works on silicon diodes for bolometers [2][3][4], we investigated the performances of vertical short diodes made with epitaxial silicon junctions.

II. FABRICATION

Initially, 50-nm Silicon-On-Insulator (SOI) wafers produced with Smart Cut are used. Starting from the SOI substrate, successive epitaxies by RTCVD are made in order to obtain p^+pn^+ diodes. Once the epitaxies are completed, the shape and size of the diodes are fixed by dry etching. The sizes range from 1 to 10 µm (Z). A first contact is created. Then, the structure is put face to face and bonded onto a second wafer. Finally, a second contact is achieved by etching the silicon and the Buried oxide of the original SOI wafer. In the structure, we admit different types and sizes (C) for the contacts that are displayed on Table 1. A schematic cross section of the structure of the diodes is represented on Figure 1.

III. RESULTS AND DISCUSSION

At 303-353 K, electrical characterizations are done using B1500A Semiconductor Device Parameter Analyzer to extract the Temperature Coefficient of Current (TCC) : $TCC = \frac{1}{I}\frac{dI}{dT}$. Figure 2 presents these results at 303 K. The TCC has a similar evolution for all the diodes and is in agreement with previous works [2]. At 303 K and 0.6 V, it takes a value between 4.6 and 6.2 %/K. The Power Spectral Density (PSD) of the current noise S_i is measured using a Dynamic Signal Analyzer HP35670A. We observed that S_i is dominated by flicker noise (Figure 3) and proportional to I^k with 1< k < 1.66 (Figure 4). Our hypotheses are that the noise comes from the bulk and corresponds to different sources of noises (mobility fluctuations 1/f noise and generation-recombination noise) related to the epitaxial processes [5]. We calculate the thermal resolution (ΔT_{min}) of our diodes (K) : $\Delta T_{min} = \frac{i_n}{TCC \times I}$. i_n is the root mean square (RMS) current noire (in A) of S_i. At 303 K and an integration time τ_{int}= 60 µs, a ΔT_{min} between 2.10^{-3} and 5.10^{-2} *K* is found for currents at 10^{-9}-10^{-5} A (Figure 5). For the same current range and at 300 K, *Fournol et al.* found a ΔT_{min} between 6.10^{-4} and 5.10^{-3} *K* [2] and *Corcos et al.* between 8.10^{-3} and 5.10^{-2} *K* [3].

IV. CONCLUSION

Epitaxial p+pn+ short diodes were successfully fabricated and characterized at 303-353 K. The thermal resolution ΔT_{min} of the diodes were estimated. We obtain a value between 2.10^{-3} and 5.10^{-2} *K* for bias currents ranging from 10^{-9} to 10^{-5} A at 303 K. It shows promising performances for future microbolometers.

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V. ACKNOWLEDGMENT

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Table 1 : Characteristics of studied diodes

Name	Z (µm)	C (µm)	Number of contacts
D1	1	0.5	1 x 1
D2	2	0.5	1 x 1
D3	6	0.5	1 x 1
D4	6	5.1	7 x 7
D5	10	9.1	12 x 12

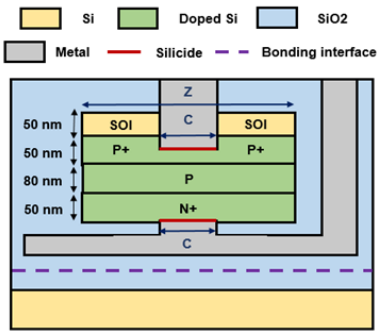

Figure 1 : Schematic cross section of the structure of the diodes.

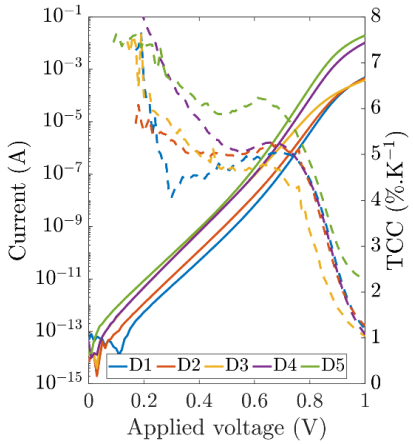

Figure 2 : IV characteristics (solid line) and TCC (dashed line) of the diodes as a function of the applied voltage at 303 K.

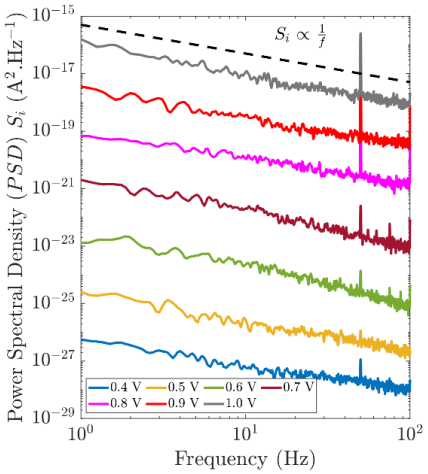

Figure 3 : PSD of the current noise (Si) of D1 for different applied voltages as a function of the frequency (Hz) at 303 K.

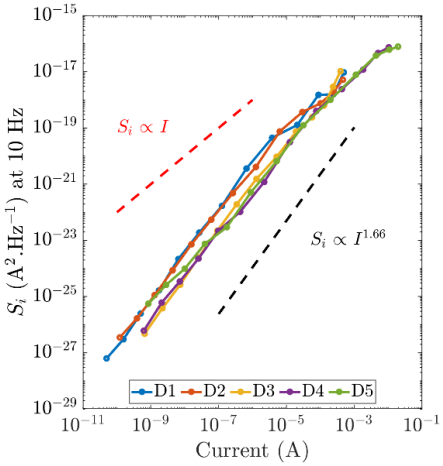

Figure 4 : PSD of the current noise (Si) as a function of the current (A) at 303 K and 10 Hz.

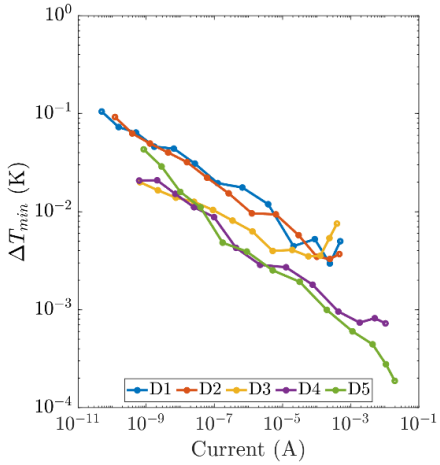

Figure 5 : The thermal resolution ΔTmin as a function of the current (A) at 303 K.

Engineering Thin HZO Ferroelectric Layers: From Material Study to 3D Integration for Vertical Gate-All-Around FeFETs

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The demand for higher computational efficiency and lower energy consumption in semiconductor devices has led to the exploration of non-traditional computing architectures. One promising direction is the integration of logic and memory into a single device or cell, potentially overcoming the limitations of the Von Neumann architecture. This paradigm is now within reach thanks to the introduction of CMOS compatible ferroelectric materials, such as hafnium oxide (HfO_2), known for its reversible residual polarization under the effect of external electric fields[1].

This study presents a thorough investigation of the Hf-Zr ($Hf_{0.5}Zr_{0.5}O_2$ - HZO) layer and the subsequent steps towards its integration into 3D gate-all-around devices [2], currently targeted for the next technology nodes in logic architecture. Fig.1 shows planar MIS devices, with a 10nm HZO layer, that display through GIXRD the successful crystallization of HZO with annealing temperatures starting as low as 400°C. The ferroelectricity and thus the orthorhombic crystalline phase of HZO is verified through pulsed electrical measurements which exhibit a robust (P-E) hysteresis loop. Integration on vertical nanostructured channels has been successfully demonstrated (Fig. 2) with a perfect conformity of the layer. In a 3D nanoscale configuration, identifying the proper ferroelectric phase with classical approaches (such as GIXRD) used in planar structures is not feasible. So, we developed a novel approach that couples 4DSTEM imaging and python based data processing to perform a full mapping of the grains and crystalline phases of our HZO layer.

Furthermore, we investigate the challenges related to integrating the HZO layer into 3D nanostructures, particularly selective and anisotropic etching steps, to maintain the integrity of the HZO layer (see Fig. 2). This ensures the removal of unwanted layers from our nanostructures while preserving the surrounding HZO layer, facilitating the subsequent formation of alloy contacts. Additionally, considering the opportunities and possible limitations of fabrication parameters, we explore different process routes in parallel (S/D contact first/last) for the 3D integration of HZO in gate all-around FeFETs (see Fig. 3), discussing the pros and cons of each configuration (metallurgy stability of the contacts, doping segregation at the interfaces etc).

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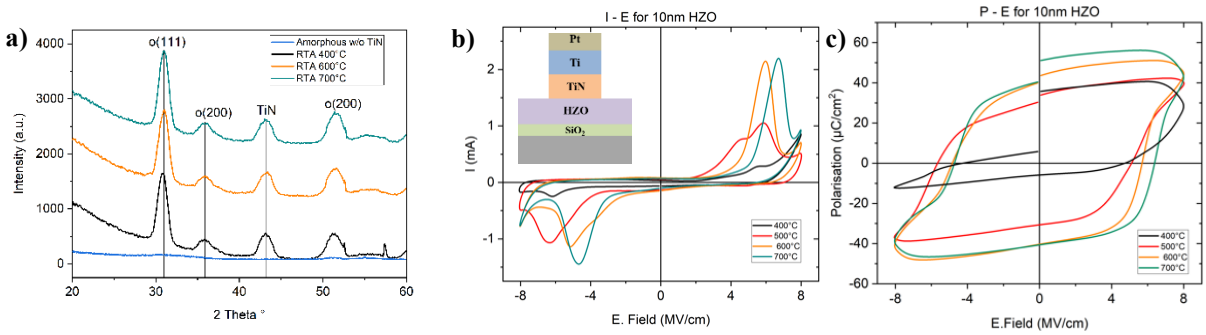

Figure 1: (a) GIXRD verification of the crystalline nature and identification of the orthorhombic phase on our planar samples. The electrical measurements were conducted on a stack of 1.5nm of SiO_2 on Si substrate followed by 10nm of HZO, 13nm of TiN and a total of 35 nm of Ti/Pt as top contact. Results of I vs E_{field} (b) and P vs E_{field} (c) demonstrate the evolution of polarization and Ec for different HZO activation annealing temperatures.

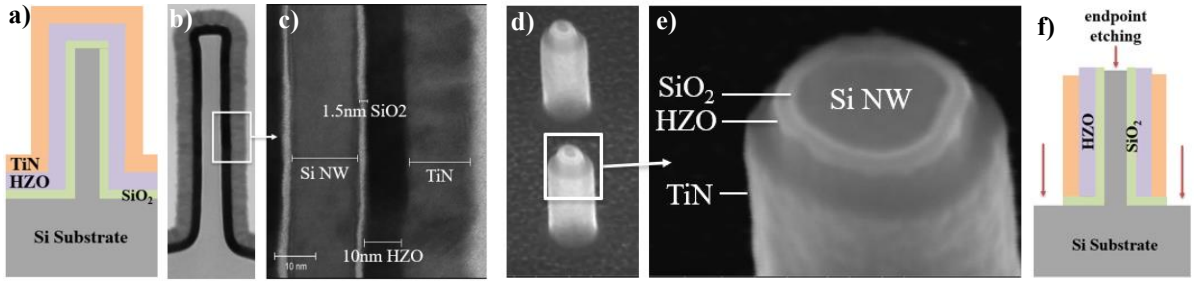

Figure 2 : (a)Schematic of the vertical HZO/TiN deposition. (b) TEM from vertical nanowire with crystalized SiO2/HZO/TiN multistack with a (c) zoomed view on the critical sidewall. (d)birds view SEM plasma etched vertical nanowires where TiN/HZO have been removed from (e) top and bottom with the corresponding 2D sketch(f)

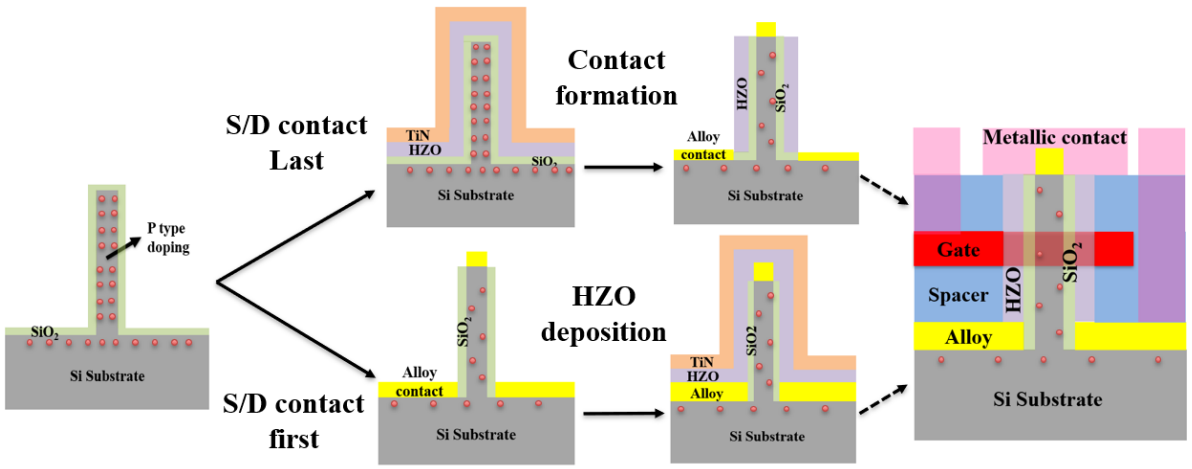

Figure 3 : The two different fabrication approaches process flow of a Vertical Nanowire GAA FeFET (S/D contact first/last). The red dotes demonstrate the p type doping. The stabilization and integrity of the formation of the alloy contact is critical in order to ensure good electrical properties of the transistor.

This work was supported by European Union's H2020 program through the FVLLMONTI project (N◦101016776) and the Renatech French national network

Si/$Ge_{1-x}Sn_x$/Si transistors with highly transparent Al contacts

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The introduction of GeSn as a channel material, with its modulated band structure and high carrier mobilities for both electrons and especially holes, is promising for optoelectronics and Beyond- CMOS technologies with high on-state conductance as well as low power cryogenic applications. [1] Therefore, forming high-quality contacts to the GeSn is of utmost importance. In this regard, we investigate the Al contact formation to nanosheets composed of thin $Ge_{1-x}Sn_x$ layers with Sn concentrations from 0.5% to 4%. The nanosheets are patterned from vertical Si/$Ge_{1-x}Sn_x$/Si heterostructures (Fig. 1), grown on SOI substrates by molecular beam epitaxy (MBE) at ultra-low temperatures of 175°C, adapted from the SiGe growth in [2]. Utilizing a thermally induced exchange reaction [3] between Al and Si/$Ge_{1-x}Sn_x$, monolithic metal-semiconductor-metal lateral heterostructures with abrupt Al-$Ge_{1-x}Sn_x$ junctions are formed (Fig. 2). Implemented in field-effect transistors, the electrical transport is investigated (Fig. 3), revealing linear IV-characteristics, suggesting highly transparent quasi-ohmic contacts. The transfer characteristics show a very dominant p-type conduction, which can be attributed to strong Fermi level pinning to the valance band and potentially also to hole-gas formation between the 4 nm thin $Ge_{1-x}Sn_x$ layer sandwiched vertically between two Si layers.[3] Temperature-dependent measurements indicate that at cryogenic temperatures, the $Ge_{1-x}Sn_x$ channel can be sufficiently depleted due to fewer thermally excited states at $V_G > 0$. This results in a drain current modulation over three orders of magnitude, while the on-currents remain mostly temperature-independent, making the system especially interesting for cryo-CMOS applications. The comparison of nanosheets with different stoichiometries (Fig. 4) shows that an increased Sn content enhances conductivity, over 20x higher vs. a control sample with a pure Ge layer in agreement with an accumulation channel. However, the off-state is given by depletion implying a V_G dependent overall gate capacitance accompanied with degraded I_{on}/I_{off} ratios and subthreshold slopes. To decouple the influence of the carrier injection barrier and the channel conduction, a multi-gate structure, featuring a junction gate (JG) atop the Al- $Ge_{1-x}Sn_x$ interfaces and a channel gate (CG) in the middle of the $Ge_{1-x}Sn_x$ channel, is investigated (Fig. 5). Thereby, it was found that keeping V_{JG} at -5 V and sweeping V_{CG}, the on-state resistance can be improved by a factor of ~40.

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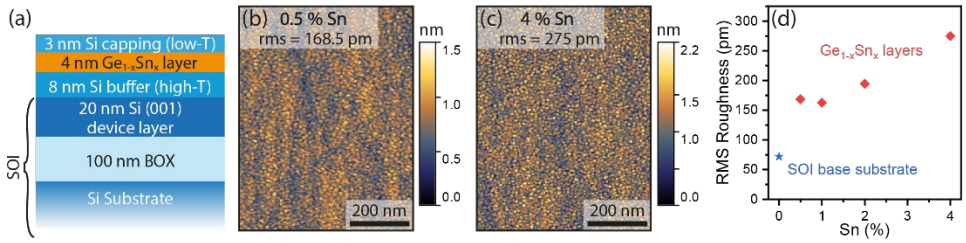

Fig. 1: (a) Schematic of the epitaxially grown Si/$Ge_{1-x}Sn_x$/Si heterostructure on SOI, with AFM surface topography of the substrate containing 0.5% (b) and 4% Sn (c). The root-mean-square surface roughness of four substrates with different Sn contents (0.5%, 1%, 2%, 4%) and the base SOI substrate are compared in (d).

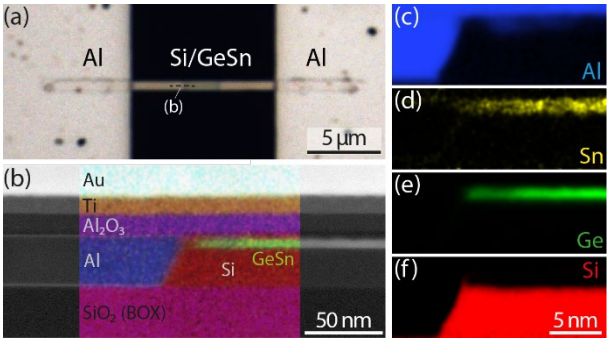

Fig. 2: (a) Microscope image of the formed Al-Si/$Ge_{0.99}Sn_{0.01}$ heterostructure after the thermally induced exchange reaction. (b) HAADF-STEM image with EDX overlay of the axial cut at the Al-Si/GeSn interface, indicated in (a). (c)-(f) Single elementary EDX maps.

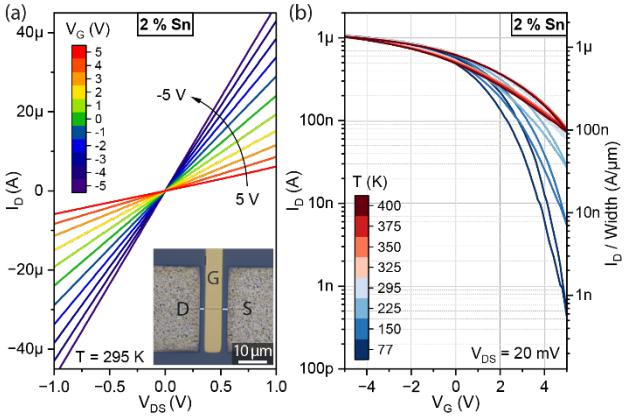

Fig. 3: (a) Linear gate dependent I/V characteristic of a top-gated Al-$Ge_{0.98}Sn_{0.02}$ heterostructure shown in the inset. (b) Temperature dependent transfer characteristic at V_{DS} = 20 mV.

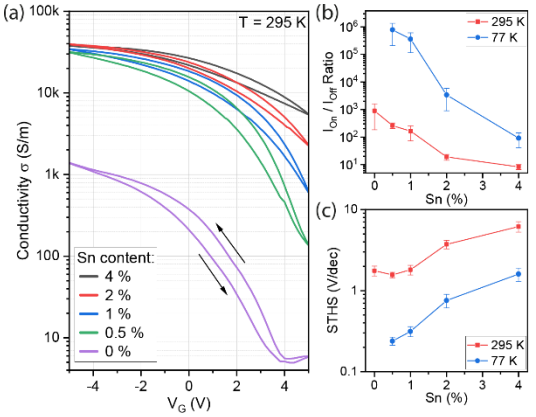

Fig. 4: (a) Comparison of the gate dependent conductivity of samples with different Sn content, including a reference sample with a pure Ge layer. (b) I_{on}/I_{off} ratio and subthreshold slope (STHS) vs Sn content, at 295 K and 77 K.

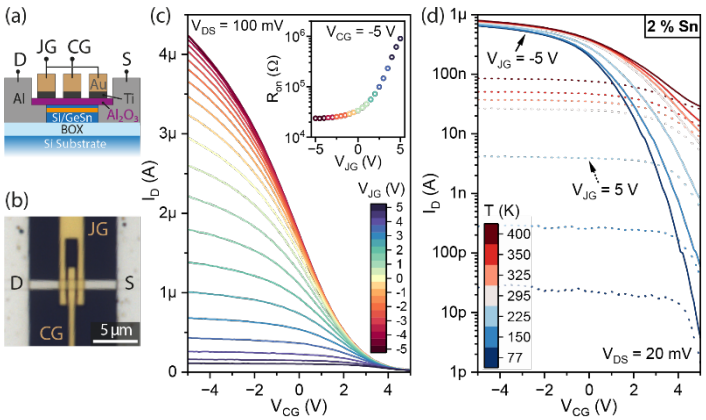

Fig. 5: (a) Schematic and (b) microscope image of a multi-gate structure with 2% Sn. Junction gate (V_{JG}) dependent transfer characteristic, with the inset showing the change in on-state resistance (R_{on}). (b) Temperature dependent transfer characteristic for V_{JG} = -5 V (solid) and V_{JG} = 5 V (dotted line).

Temperature-Dependent Electronic Transport in Reconfigurable Transistors based on Ge on SOI and Strained SOI Platforms

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Reconfigurable field-effect transistors (RFETs) allow the dynamic switching between n- and p-type operation during run-time. RFETs have been identified as add-on technologies to CMOS, that can efficiently map XOR and majority gate logic, provide hardware security primitives and analog circuits for sensor front-end.

To boost performance and switching power efficiency vs. Si, Ge has been predicted as the RFET channel material of choice. However, the complex junction and oxide interface formation have so far hindered hysteresis-free operability and providing high as well as the necessary symmetric on-state- with reasonable off-state currents between both n-/ p-type IV characteristics [1],[2]. Here we bypass these aspects, [3] first by growing Ge on top of a <110> SOI substrate by low-temperature molecular-beam epitaxy, constituting our Ge on SOI (GeSOI) platform. To obtain thicker and more relaxed Ge layers, a strained-Si on insulator (s-SOI) platform was established (see Fig. 1a,b). As evident in the transfer characteristic shown in Fig. 1, the GesSOI platform exhibits higher on-state currents normalized to the cross-section, lower threshold voltage (V_{th}) but also relatively slightly higher on-state asymmetries compared to the GeSOI platform, while both retain a neglectable off-state current. Nevertheless, both platforms provide stable regimes of operability, as outlined in Fig. 2 for the GesSOI RFET, considering the gate-voltage-dependent switching capabilities. Consequently, the elaborated operational stability of these device platforms allows to investigate temperature-dependent IV characteristics, from which the transport regimes and activation energy for the RFETs can be extracted. In this respect, to give a comprehensive picture of the influence of the different parameters on the transport mechanisms, temperature-dependent gate- and bias-dependent current-voltage data was evaluated constructing 2-D colormap representations, as shown in Fig. 3 und Fig. 4 for the GeSOI and GesSOI platform, respectively.

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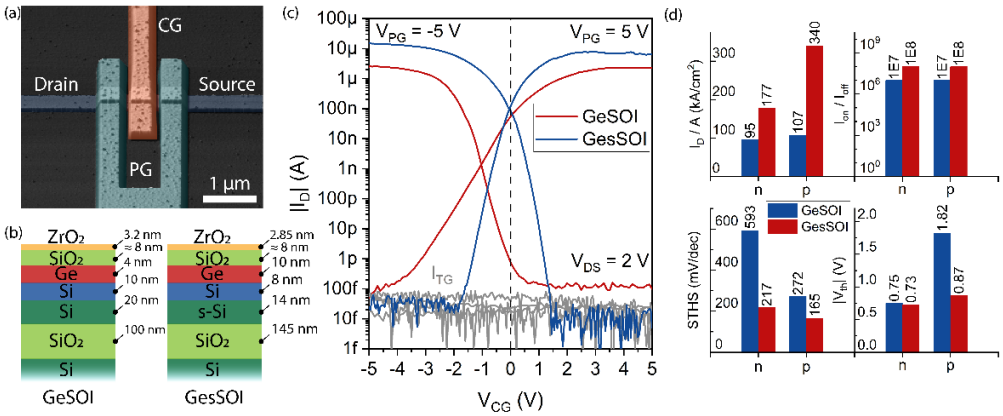

Fig. 1: (a) False-color AFM scan of the triple-gated RFET. (b) Schematic of GeSOI and GesSOI platform stacks. (c) Corresponding transfer characteristic of the RFET devices for both platforms, where the mode is set with a PG voltage V_{PG} of 5V for n-type and -5V for p-type operation and a symmetrically applied bias V_{DS} of 2V (V_D = 1V, V_S = -1V) (d) Transistor parameter evaluated for the shown devices of both platforms.

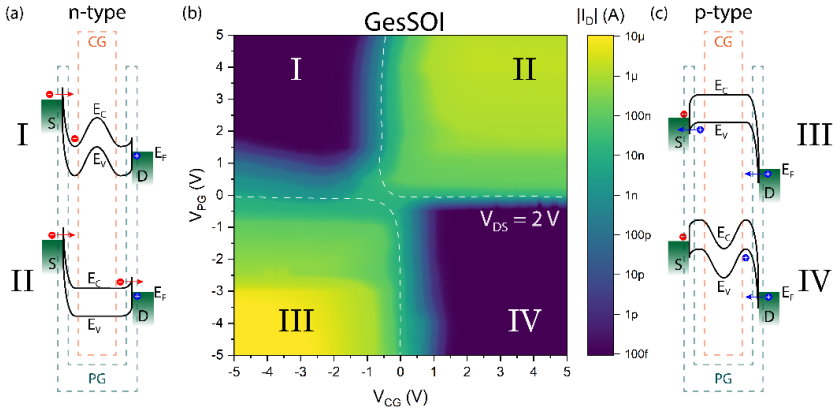

Fig. 2: Gate-voltage-dependent switching capabilities of the GesSOI platform (b) with the corresponding band diagrams and the related band bending situation for both operation modes, for n-type (a) and p-type (c).

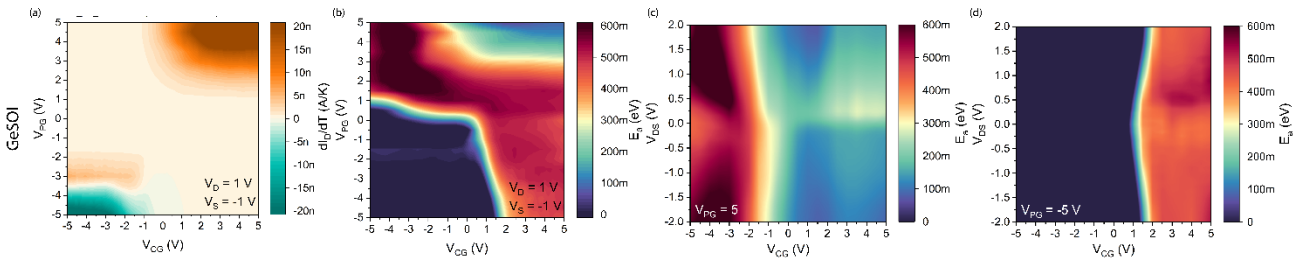

Fig. 3: Gate-voltage-related (a) temperature gradient for GeSOI RFETs and (b) activation energy for GeSOI RFETs for a constant bias. Bias-related and CG-dependent activation energy for n-type (c) and p-type operation (d) for the GeSOI platform.

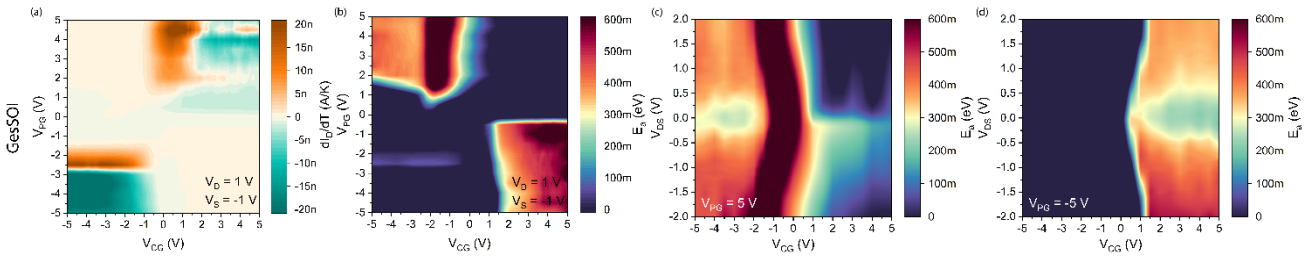

Fig. 4: Gate-voltage-related (a) temperature gradient for GesSOI RFETs and (b) Gate-voltage-related activation energy for GesSOI RFETs for a constant bias. Bias-related and CG-dependent activation energy for n-type (c) and p-type operation (d) for the GesSOI platform.

Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: transistor performance recovery and back gate bias influence

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Resistive Switching (RS) phenomenon has acquired a lot of interest in the scientific community because its potential use in many applications such as memory, logic, security, neuromorphic systems, etc [1]. Devices where RS is observed are usually named as memristors and, after a forming process, RS provokes a reversible change in the device dielectric conductance between a high and a low resistance state (after a set process) and vice versa (reset process) when a correct bias is applied (Fig. 2B). Usually, memristors are two-terminal capacitive structures, but RS has also been observed previously in FD-SOI quasi-planar transistors [2]. The RS observation in transistors opens the possibility of using the device in a versatile mode as transistor or memristor, as necessary [3]. In this work, for the first time, partial recovery of the transistor characteristics during RS is investigated in N-type FDSOI Ω-gate nanowire FETs with high-k dielectric. On the other hand, other works have observed the influence of the back gate voltage (V_B) in the main parameters of Ω -gate nanowires transistors [4-6], but none of them have analyzed the effect of this biasing on RS, so that, in this work it is also investigated the influence of V_B on RS.

The Ω-gate NW-FETs used in this work were fabricated at CEA-LETI with SOI (Silicon on Insulator) technology, gate length L=10µm and width W=10µm [6]. Their device planar representation and cross-section are shown in Fig. 1A. and Fig. 1B respectively. The great difference between the gate dimensions compared to the nanowire height makes it to be considered as quasi planar SOI MOSFET (Fig. 1C). The electrical measurements were performed with a prober and a Precision Semiconductor Parameter Analyzer Agilent 4156C.

Fig. 2 shows the I_G-V_G measurement after forming (Fig. 2A) and during a complete RS cycle (Fig. 2B). I_D-V_D curves of the fresh sample (Fig. 2C) and after the forming (Fig. 2D), reset (Fig. 2E) and set (Fig. 2F) processes are also represented. Note that transistor functionality is partially recovered after the reset process under the applied electrical conditions (see Fig 2 caption). Fig. 3 shows several RS cycles, obtained with V_B=0V (Fig.3A) and V_B= - 0.2V (Fig.3B). The I_{on}/I_{off} mean ratio calculated at V_G = -1V (see Fig.3A) is 20.08, and 77.9 respectively. This I_{on}/I_{off} ratio increase for larger V_B (in absolute value) improves the distinction between the memristor conduction states, which is beneficial for memory applications.

In summary, this work experimentally studies on the one hand, the I_D-V_D transistor curves during RS stages, which have been partially recovered after the reset process when applying the adequate RS voltages and current limit conditions. This demonstrates the possibility to implement together in a single device a memristor and a transistor. On the other hand, the experimental study of the back gate voltage influence on RS shows that the I_{on}/I_{off} ratio increases with V_B. Future works will explore in more detail these preliminary results.

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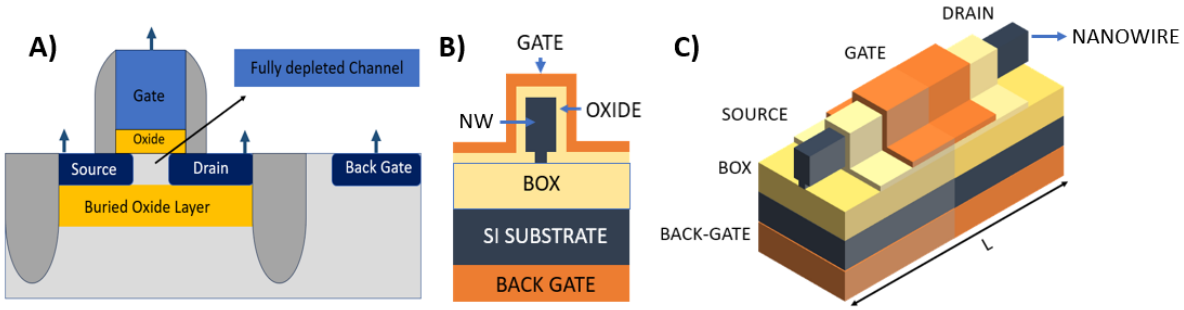

Figure 1. Planar representation of the FD-SOI FET (A) cross section of the Ω-gate Nanowire (B) 3D sketch (non in scale) of the FD-SOI quasi-planar transistors used in this work (C).

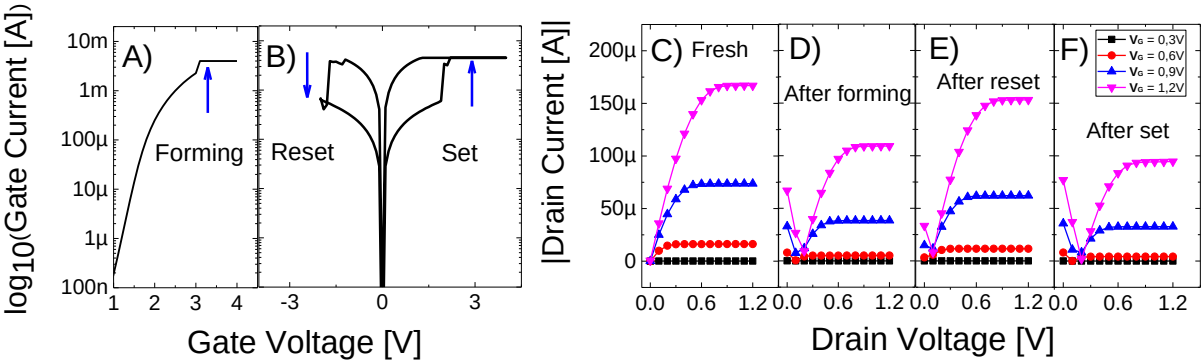

Figure 2. Experimental I_G-V_G curves for A) 'forming' (V_G = 0 to 4V and current limit= 4mA), B) 'reset' (V_G = 0 to -2V and current limit= 8mA) and 'set' (V_G = 0 to 4V and current limit= 4.5mA) processes. I_D-V_D transistor characteristics (V_D = 0 to 1.2V) when (V_G = 0.3V, 0.6V, 0.9V to 1.2V) C) for fresh device. D) after forming. E) after reset and F) after set processes.

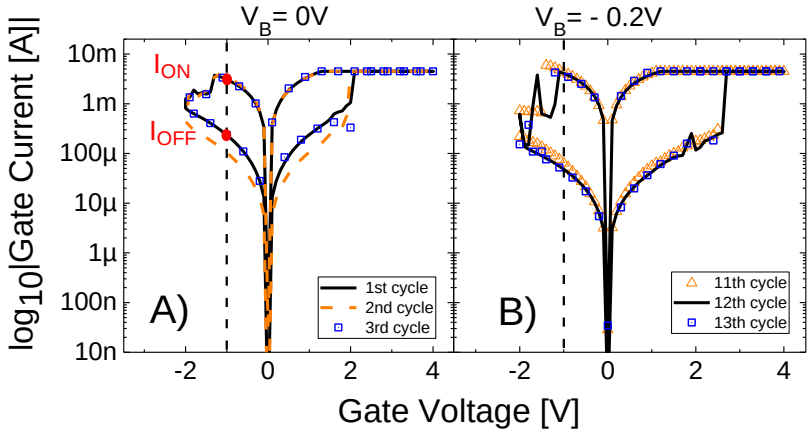

Figure 3. I_{ON}-I_{OFF} ratio measured when A) V_B= 0V, B) V_B= -0.2V.

Preliminary results on industrial 28nm FD-SOI phase change memory at cryogenic temperature

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Abstract:
This study reports new preliminary results on pulse programmed 28 nm FD-SOI UTBB fully co-integrated phase change memories (PCM) at room (RT) and cryogenic temperatures (CT). The PCM is found to be functional at 77K featuring multi-state switching with no extra operating requirements compared to RT. As the phase change memory is temperature dependent, drift tests are carried out to track the resistance change overtime subsequent to pulse programming to estimate the drift coefficients. A striking feature is that using the same programming conditions, the drift coefficient is 3 times lower at 77K with improvement on I_{on}/I_{off} ratio. These results are encouraging and open the door for PCM in cryogenic applications.

Keywords- FD-SOI CMOS, phase change memory, cryogenic temperatures

I. INTRODUCTION

In the fields of quantum, avionics, space applications or detectors in astrophysics/medicine and accelerators, cryogenic temperature is a key parameter with a wide low temperature range down to mK. Depending on the system architecture and temperature distribution, the choice of electronic control technology is very important. One of the promising candidates is FD-SOI technology which today demonstrates relevant performances, particularly in low power consumption, for analog/digital design. That's why 28nm platform devices are based on STMicroelectronics' standard 28nm ultra-thin body buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) technology. These devices are explored under cryogenic temperature conditions. Thus, the industrial process has been shown to be functional down to 20 mK without additional process steps. Figure 1 recalls the thin hybrid silicon film substrate and gives the $I_{ds}(V_{gs})$ from room temperature to 20 mK. This demonstrates the exceptional subthreshold slope around 2 mV/decade at 20 mK. It is also reported that the thermal offset Vt is corrected by the back gate control for P and NMOS transistors. Additionally, Phase Change Memory (PCM) is offered in the platform to deliver emerging non-volatile memories (eNVM) functionality. Figure 2 gives the design principle of 1T1R memory, a typical PCM layout where an SEM cross section represents the architecture and material types. Additionally, the phase of the material is also shown to highlight the forming, set and reset configuration based on electronics set up control. After this overview of the context, the novelty of this study is to demonstrate that with the initial configuration, it is possible to program the PCM in binary and/or multilevel mode at cryogenic temperature with no extra operating requirements. For this first investigation, the thermal condition selected is 77K. Figure 3 gives several views of the cryo-probe station test setup and the pulse programming scheme used to perform multilevel switching by means of a Keysight (Agilent) B1500A Analyzer. Binary states (high resistance state (HRS) and low resistance state (LRS)) and intermediate states are obtained at room temperature. The incremental switching using the programming sequence depicted in figure 3 consists of 10 constant amplitude SET pulses of 1.5V and 10 subsequent RESET pulses with incrementing amplitudes ranging from 1.8V to 2.7V. The pulse format remains consistent for both set and reset, with uniform rise, plateau, and fall times of approximately 70ns. The sequence is executed across BL with a steady 1.3V bias applied to WL. Each pulse is followed by 0.1V reading pulse. Figure 4a) and b) present the IV DC sweep measurements at HRS with fixed V_{WL} bias at RT (300 K) and at 77K. The corresponding fitting of Poole-Frenkel conduction dependence is also presented. As expected, we observe a considerable increase in HRS at cryogenic temperatures. Next, the set/reset incremental pulse programing sequence is applied to reach four states at RT and CT. The density distribution of resistance states achieved with 4 selected different programming steps over more than 100 pulses are reported in figure 4. Although the LRS range is the same regardless of the temperature, the HRS and intermediate resistance states (IRS) are higher at 77K Thus, it is possible to reduce the V_{BL} voltage requirements at 77k and still obtain the same resistance range and ON/OFF ratio as at RT that conversely requires a voltage of 2.7V to reach full switching range. This means that standard thick gate oxide MOS transistors could be used for the design of the selector. Figure 5 shows the temporal evolution of PCM resistance after programming and the drift model used to extract the drift coefficients (υ) of the four-state resistance at RT and 77k. Note that the states are read at 0.1 V to avoid additional self-heating in cryogenic conditions compared to 0.2 V. The drift is reduced by 3 times at 77K compared to the thermal condition of 300K. In conclusion, we report for the first time the demonstration that it is possible to program and read the PCM performing binary or multilevel switching with the same standard set up configuration at 300K and 77k. Additionally, the 28 nm FD-SOI PCM demonstrates reduced drift at cryogenic temperatures(77K). It is recalled here that this PCM (GST type) is manufactured using an industrial steps process. This study opens the door to push the limit of the cryogenic temperature where the eNVM proves to be functional. The same trend is expected to be observed on next generation nodes, for example in 18nm.

ACKNOWLEDGMENTS

The authors of this article would like to thank all colleagues at STMicroelectronics and 3IT/IQ who contributed to these results within the standard 28 nmFD-SOI process.

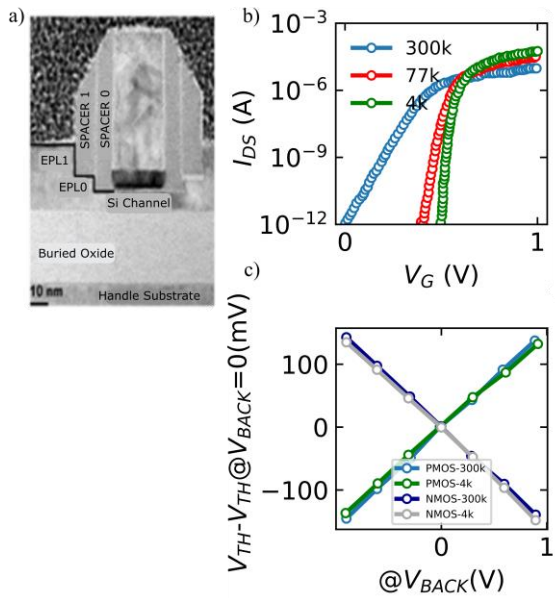

Figure 1: a) FD-SOI substrate cross section, b) $I_{ds}(V_{gs})$ for various temperatures down to 4K and c) Back Bias V_T correction for N/P MOS transistors.

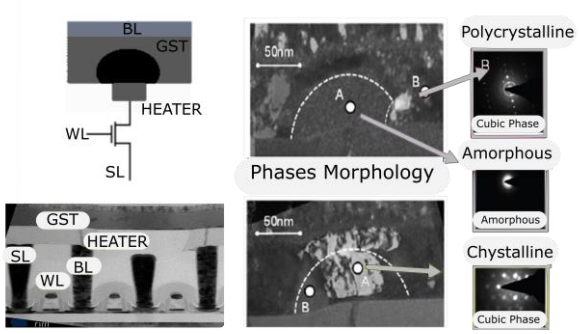

Figure 2: a) 1T1R PCM (GST material), typical Layout in 28 nm FD-SOI. PCM phases and wall PCM SEM cross section with heater and contact are depicted.

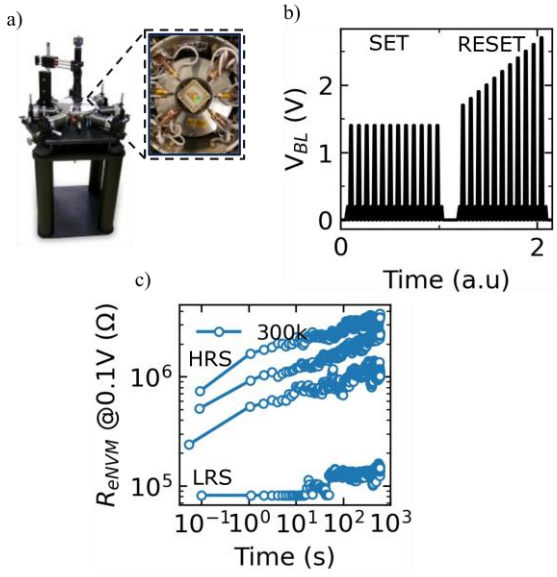

Figure 3: a) Cryogenic test setup for b) incremental set/reset pulse programming. c) Time retention at 300k up to 600s for four multilevel states corresponding to a set of selected steps within the entire programming sequence consisting of 10 SET and 10 RESET pulses (average across 10 complete sequence repetitions) (at RT.).

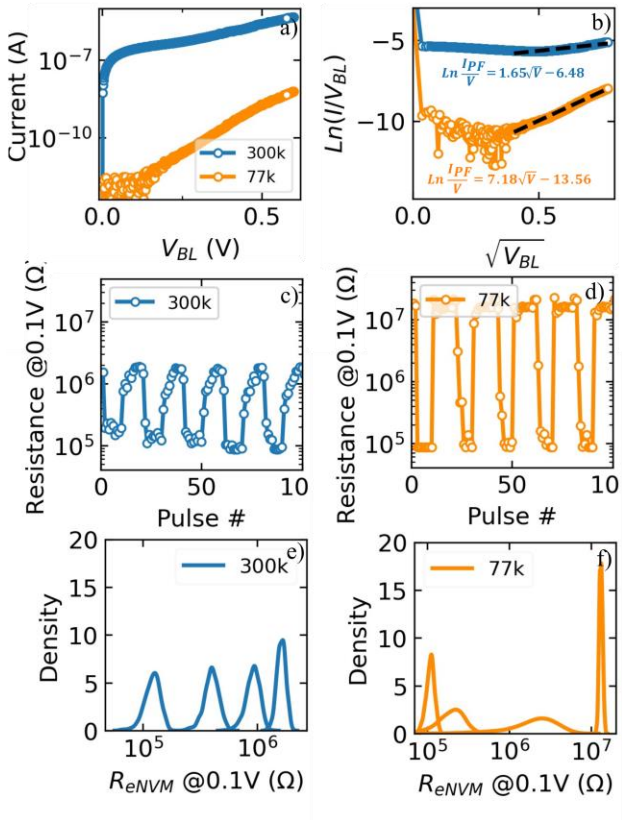

Figure 4: a) PCM IV DC sweep measurements at 300K and 77K (@HRS) and b) the corresponding fitting of Poole-Frenkel conduction dependence; c) A resistance sequence is pulse-programmed at both 300K and d) 77K, e) depicting the multilevel resistance states distribution for four selected programming steps repeated over time at 300k and f) 77k.

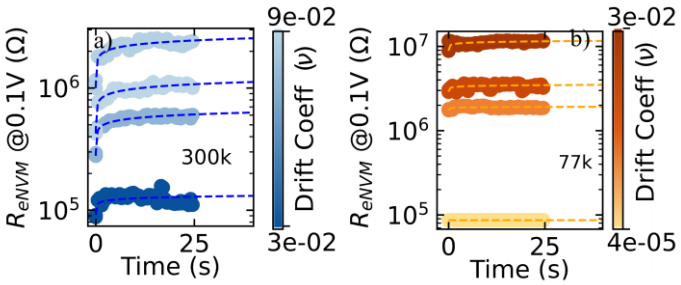

Figure 5: Time retention measurements and drift coefficient (ν) estimation according to drift model $R_t = R_{t0}(t/t_0)^{\upsilon}$ for 4 different states programmed at a) 300 and b)77K. First reading t_0 is at 0.9ms.

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Investigation on the Performance Limits of Dirac-Source FETs

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Introduction. The investigation in the area of steep-slope FETs was recently enriched by a proposal exploiting the conical band structure of graphene to control high-energy electron injection into the channel of a 2D-material based FET [1-4]. In this work, we extend the approach adopted in [3-4] by developing a two-dimensional (2D) simulation tool addressing Poisson's equation within the MoS_2 section of the DS-FET under the assumption of ballistic transport. Next, we compute the device characteristics, which are quite sensitive to the tunneling probability at the graphene-MoS_2 heterojunction. Our results confirm that a subthreshold swing SS as low as 40 mV/dec can be achieved, and that SS values below 60 mV/dec are extended up to three and a half decades.

Simulation approach. We assume a zero thickness of the semiconductor monolayer and, thus, a delta-like electron distribution. With this approach, we just need to solve Laplace equation within the oxide and use the charge density per unit area to establish the appropriate nonhomogeneous Neumann boundary condition at the semiconductor interface. As the charge density depends on the local potential, an iterative procedure is required to solve the problem. Both an SOI and a DG-FET can be treated by the code. The device characteristics are computed using Landauer's formalism with the WKB approximation for the tunneling probability. The current integration is carried out numerically on the 2D potential profile. It's worth noting that the device performances are influenced by the energy difference between the barrier height at the graphene-channel heterointerface and the Fermi level in graphene source $\phi_{SB} = E_C(0) - E_{FS}$.

Simulation results. In this investigation, the Dirac energy below the graphene control gate is set at 0.3 eV, leading to a leakage current I_{OFF} slightly below 10^{-9} A/μm at $V_{GS} = 0$ V. Fig. 1 shows the MoS_2 conduction band profiles in the transport direction for two gate lengths, namely: $L_g = 10$ nm (solid lines) and $L_g = 3$ nm (dashed lines) and different gate voltages. In both cases, a 1-nm SiO_2 gate insulator is considered. Dotted lines refer to an HfO_2 gate insulator device with the same equivalent oxide thickness (EOT). Fig. 2 represents the turn-on characteristics of the DS-FET for different values of ϕ_{SB} (solid lines). The dashed lines represent instead the device characteristics computed with the assumption of a triangular barrier with a 4-nm base width, as was done in Ref. [3]. The figure shows that the ON-state current is heavily underestimated with such a simplified potential behavior, especially for the highest energy barriers. Fig. 3 shows the turn-on characteristics and subthreshold-swing (SS) for the SiO_2 (solid lines) and for the HfO_2 (dashed lines) gate-insulated DS-FETs. Finally, Fig. 4 exhibits the turn-on curves for two different DS-FETs with gate length $L_g = 10$ nm (solid lines) and $L_g = 3$ nm (dashed lines) and the minimum SS as a function of gate length.

Conclusions. This study proves that an accurate 2D potential profile is a prerequisite for a quantitative prediction of the DS-FET potential in view of future practical applications and shows that an SS below 40 mV/dec can be achieved and sustained over 3 to 4 orders of magnitude of currents.

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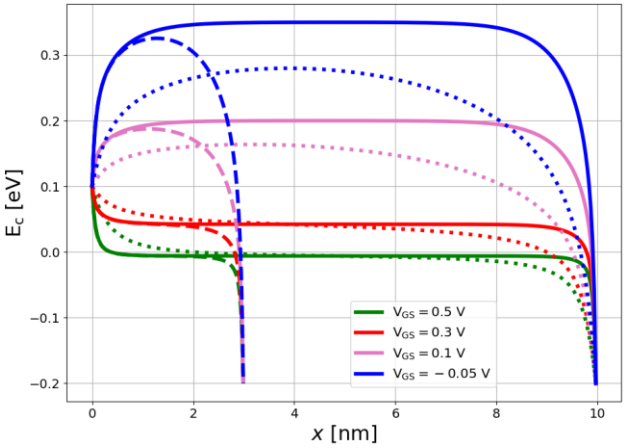

Fig. 1. Conduction band profiles in the lateral direction for two gate lengths, namely L_g = 10 nm and L_g = 3 nm and different gate voltages, ranging from -0.05 V to 0.5 V. ϕ_{SB} = 0.1 eV is assumed. Solid lines refer to a SiO_2 gate insulator having a thickness t_{ox} = 1 nm; dotted lines refer to an HfO_2 gate insulator with the same EOT. A substantial lowering of the potential barrier occurs within the channel at low gate voltages with the HfO_2 dielectric.

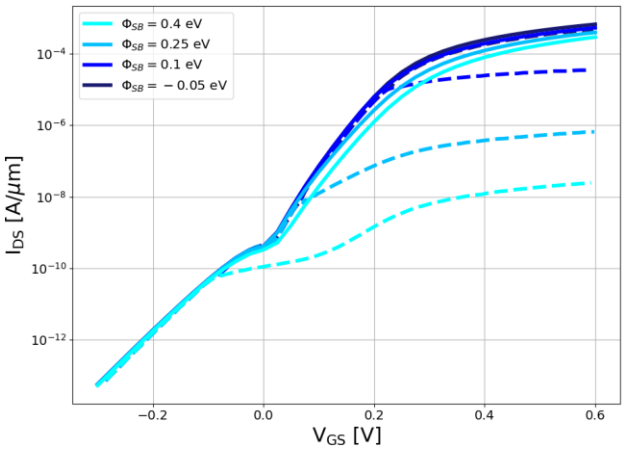

Fig. 2. Transfer characteristics of the DS-FET with a gate length L_g = 10 nm and a SiO_2 gate dielectric for different ϕ_{SB} values. Solid lines: present model. Dashed lines: Tunneling probability computed with the assumption of a triangular tunneling barrier with a base width of 4 nm [3]. Assuming a fixed tunneling barrier width clearly leads to an underestimation of the current, as it overstates the actual tunneling width, as shown in Figure 1.

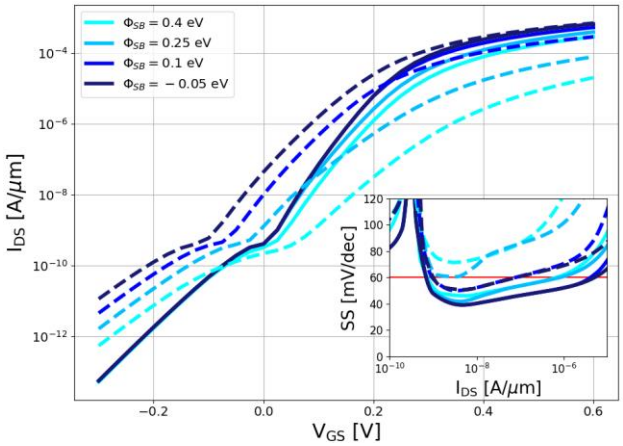

Fig. 3. Transfer characteristics of the DS-FET with a gate length L_g = 10 nm for different values of ϕ_{SB}. Solid lines: SiO_2 gate dielectric with thickness t_{ox} = 1 nm. Dashed lines: HfO_2 gate dielectric with the same EOT. Inset: SS comparison for the two devices. The use of HfO_2 as gate dielectric heavily degrades the subthreshold swing as well as the on-state current at the highest barrier heights.

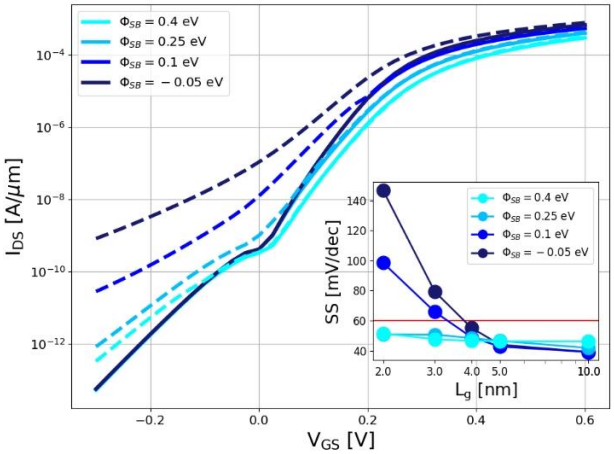

Fig. 4. Transfer characteristics of the DS-FET for two gate lengths, L_g = 10 nm and L_g = 3 nm, for different values of ϕ_{SB}. Solid lines: gate length L_g = 10 nm. Dashed lines: gate length L_g = 3 nm. Inset: minimum SS as a function of gate length in semi log axes. With low gate lengths the leakage current substantially increases and the SS degrades, as for conventional MOSFET devices.

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Impact of Device Layout on Self-heating Extraction in MOSFETs

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With increasing concerns of self-heating (SH) in advanced nodes due to higher current and power densities, reliable evaluation of SH is of increasing importance. This work analyses the impact of device layout on SH extraction and treats it in terms of parasitic series resistance and heat evacuation.

Self-heating extraction techniques: Two main techniques used for SH assessment are gate resistance [1] and RF technique [2]. The gate resistance technique evaluates SH from the temperature variation of the gate resistance using a simple DC measurement process, requiring special test structures with additional gate accesses. The RF technique, on the other hand, evaluates SH from the frequency variation of output conductance g_d and the temperature variation of drain current I_d. SH parameters (thermal resistance R_{th} and channel temperature rise ΔT) extracted by means of these techniques are often compared and the difference is attributed to the inner device features itself. However, one needs to pay attention to the fact that device configuration has an important impact on the extracted features not only due to difference in the "inner" device configuration (and thus heating and heat evacuation) but also due to different parasitic elements and heat evacuation paths. In this work we demonstrate this based on experimental data for four-terminal (4T) gate access (used for gate resistance technique) FET, complemented by PDK simulations of series resistance effect.

Devices under study: The core FET is an nFET with total width 30 µm based on 22FDX® [3]. Fig. 1 shows the layout of the 4T RF test structure (with additional DC pads/accesses to the gate) which allows to apply both gate resistance and RF techniques to the same device. This device is compared with a standard version of the RF device without the additional DC contacts.

Experimental results: The DC characteristics of the devices with 4T additional gate terminals and without them (labelled "4T" and "no 4T", respectively) are similar in terms of threshold voltage Fig. 2, allowing for a direct comparison of their SH features. Fig. 3 shows the variation of g_d with frequency (after open de-embedding) and I_d versus temperature for these FETs. Higher value of g_d and higher absolute value of $\partial I_d/\partial T$ obtained for the "4T" FET suggest that it is less affected by SH compared to the "no-4T" case. Table I summarizes the comparison of the devices from an SH perspective, showing around 20% lower R_{th} and ΔT in "4T" FET.

Discussion: Keeping in mind that the core FET ("inner" device) is the same in both configurations, we suggest that the difference in the extracted SH features arises from the different layout/accesses. Difference can arise from: (i) thermal evacuation path and (ii) parasitic series resistance. Indeed, one can expect more efficient cooling from the accesses in 4T device with "larger"/more developed heat evacuation path. This hypothesis is in line with our previous works having demonstrated that a heat sink connected to the gate of a device can reduce R_{th} [4][5] by 8-20% depending on the sink configuration/area. From a technique point of view, the actual device R_{th} is therefore underestimated due to the gate accesses themselves acting like heat sinks. Apart from that, one can suppose different series resistances in those devices, which can be either due to variability or layout related effects. Lower I_d attributed to the higher R_{sd} is seen in 4T FET in linear regime; the difference becomes smaller in saturation with heat evacuation difference coming into play (Fig. 2). Simulations using PDK model with various series resistances added to the FET reveal their effect on SH parameters extracted using the RF technique. R_s, R_d have a pronounced impact on both the g_d and $\partial I_d/\partial T$ (increasing $g_{d,LF}$ and magnitude of $\partial I_d/\partial T$)

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which is due to the difference between external applied bias and the one seen by the inner device. The impact of R_d on the g_d transition is illustrated in Fig. 4 and the corresponding change in R_{th} (Table II) is ~ 2% (in the case of low added resistances) but can go up to 7% and higher.

Conclusion: Our work demonstrates that special care needs to be taken when comparing different techniques and device configurations/layouts from SH perspective. Observed differences should not only be attributed to the inner device/techniques but also to non-negligible layout effects.

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TABLE I. MEASURED SELF-HEATING PARAMETERS ON 4T AND NO 4T DEVICE. VG=VD=0.8 V.

Device	*$g_{d,LF}$ (mS)*	*Δg_d (mS)*	*I_d (mA)*	*$\partial I_d/\partial T$ (µA/K)*	*R_{th} (Kµm/mW)*	*ΔT (°C)*
4T FET	3.46	1.69	22.7	12.11	164	99
No 4T FET	3.4	1.81	22.85	10.54	201	123

TABLE II. PDK MODEL: IMPACT OF RD ON SELF-HEATING PARAMETERS. VG=VD=0.8 V.

R_d	*$g_{d.LF}$ (mS)*	*Δg_d (mS)*	*I_d (mA)*	*$\partial I_d/\partial T$ (µA/K)*	*ΔT (°C)*	*R_{th} (Kµm/mW)*	*R_{th} Variation*	*ΔT Variation*
0 Ω	2.42	1.57	22.74	12.8	90.43	149.12	0%	0%
2 Ω	2.76	1.56	22.64	12.92	88.01	145.78	-2.24%	-2.67%
5 Ω	3.4	1.54	22.46	13.12	83.76	139.85	-6.22%	-7.37%

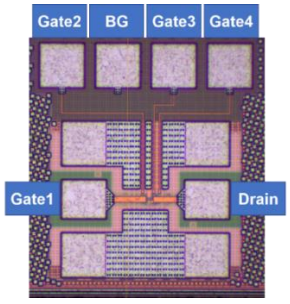

Fig. 1. 4T device layout with the two RF and four DC pads.

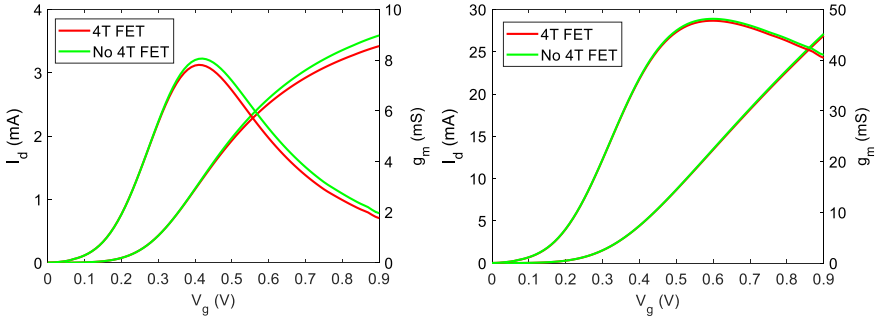

Fig. 2. I_d and g_m vs V_g for 4T and no 4T device in linear at V_d = 50 mV and saturation at V_d = 0.8 V.

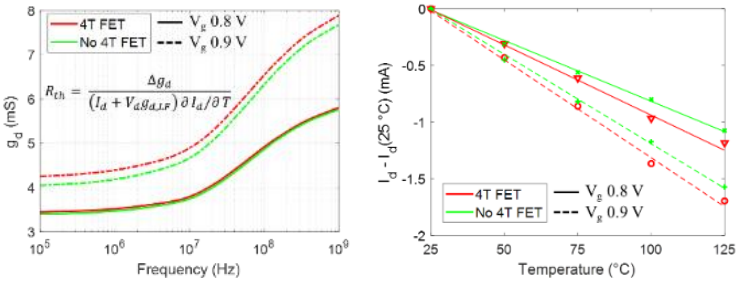

Fig. 3. g_d vs frequency and I_d vs temperature for 4T and no 4T device at V_d = 0.8 V and V_g 0.8 and 0.9 V.

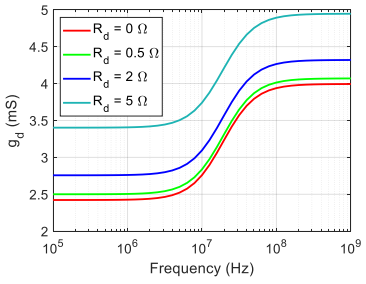

Fig. 4. g_d vs frequency from PDK model at $V_d = V_g$ = 0.8 V for varying R_d.

Operation of Junctionless Nanowire Transistors Down to 4.2 Kelvin

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Junctionless Nanowire Transistors (JNTs) appeared as an interesting alternative for MOSFET downscaling due to their less complex fabrication process when compared to standard inversion-mode nanowires associated with forming sharp junctions at the channel source and drain ends. Although several works discuss the operation of JNTs in different temperature ranges, the experimental operation of these devices in cryogenic temperatures down to 4.2K, which is of interest range for quantum computing, is scarce [1]. This work demonstrates the experimental results of state-of-the-art JNTs from 300K down to 4.2K obtained through DC measurements. The fundamental device parameters, such as threshold voltage (V_{TH}), inverse subthreshold slope (SS), low field mobility (μ_0), and Drain-Induced Barrier Lowering (DIBL) are presented and discussed.

The devices used in this work are n-type SOI JNTs fabricated at CEA-Leti, following the process of ref. [2]. Fig. 1 presents the measured drain current (I_{DS}) as a function of gate voltage (V_{GS}), obtained with a drain bias of V_{DS}=40mV for the devices with variable L and W_{FIN}=10nm for temperatures down to 4.2K. It is possible to see that all devices present a Zero Temperature Coefficient (ZTC) point in the I_{DS} *vs.* V_{GS} curves, related to the series resistance and its temperature dependence [3], indicating a reduced series resistance in the whole temperature range. The ZTC is shifted to slightly higher V_{GS} values and presents some dispersion when L is reduced [4]. Using the data from Fig. 1, the SS and V_{TH} are extracted and presented in Figs. 2 and 3, respectively. As expected, at room temperature the L reduction degrades the SS from 61mV/dec for the L=100nm to 68mV/dec for the L=20nm. For temperatures smaller than 100K, the SS difference to the theoretical limit increases and saturates at a minimum of around 10-20mV/dec at 4.2K, similarly to what is observed in inversion-mode (IM) nanowires, which can be linked to the presence of band tails at cryogenic temperatures [5]. The V_{TH}, extracted by the double derivative method, increases with the temperature reduction at a rate of $|dV_{TH}/dT|\approx$0.56mV/K regardless of the channel length between 300K and 100K, although the V_{TH} of the shorter device is always smaller. For temperatures smaller than 100K, the $|dV_{TH}/dT|$ rate appreciably reduces to about 0.003mV/K. This effect is associated with partial carrier ionization at the cryogenic regime, as the dV_{TH}/dT is directly proportional to the ionized N_D species [3]. Fig. 4 presents the extracted μ_0 as a function of temperature. For the L=100nm devices, the μ_0 increases from 60cm^2/V.s at 300K to 120cm^2/V.s at 4.2K. For the L=20nm device, the μ_0 increases from 20cm^2/V.s at 300K to 45cm^2/V.s at 4.2K. All our JNT present a clear dependence with T, regardless of L and W_{FIN}. In particular, the mobility is improved as T decreases, showing that impurity scattering is not the prevailing mechanism of transport. The mobility degradation regarding the channel length is associated with the neutral defects scattering in the channel and/or at the interface between the source and drain regions [6]. In Fig. 5 we plotted the DIBL of the studied devices, showing degradation at 4.2K with respect to 300K with different magnitude depending on L and W_{FIN}.

The junctionless nanowire transistors presented in this work have shown an appropriate behavior regarding the temperature reduction when it comes to their DC performance, with improvements in certain electrical parameters and coherent response to variations in channel length and fin width.

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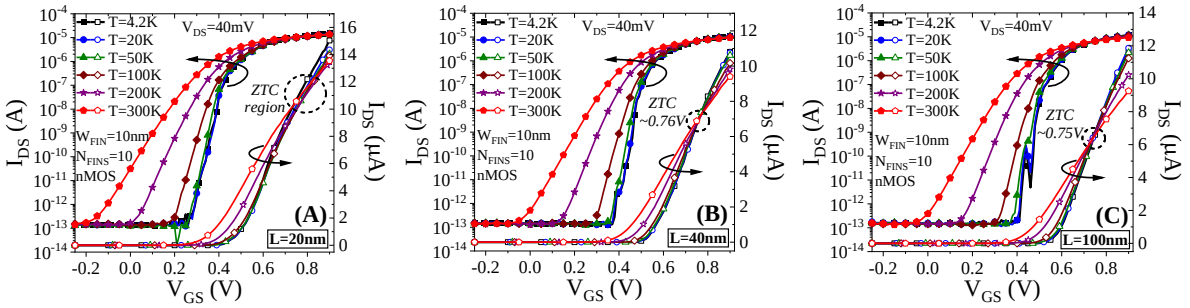

Figure 1 – Measured drain current as a function of the gate voltage, obtained with V_{DS}=40 mV, for junctionless nanowire transistors with (A) L=20nm, (B) L=40nm, and (C) L=100nm and W_{FIN}=10nm, in several temperatures from 300 Kelvin down to 4.2 Kelvin.

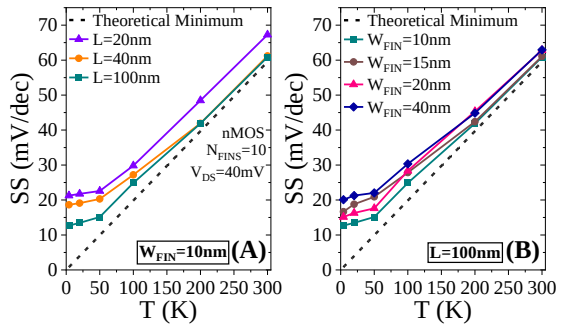

Figure 2 – Calculated subthreshold slope as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

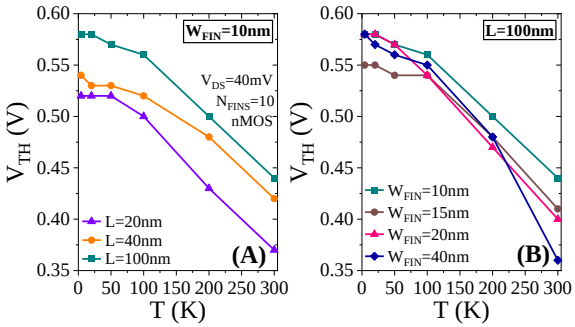

Figure 3 – Calculated threshold voltage as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

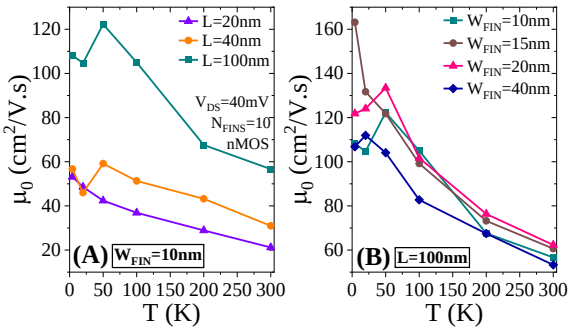

Figure 4 – Extracted low field mobility as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

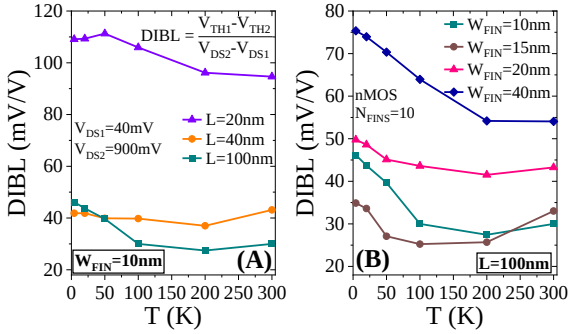

Figure 5 – Extracted drain-induced barrier lowering as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

Non-Uniform matching performances in mesa-isolated SOI MOSFETs

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Abstract— **This work studies the threshold voltage mismatch of mesa-isolated SOI pMOSFETs through a breakdown between edge and center contributions. Pelgrom's law is followed if a proper care is taken in the Vt extraction method. Applied to pMOS devices we observed that despite its parasitic nature, the edge transistor mismatch is as good as that of the center, regardless of channel doping. Even more, the edge mismatch appears to be less degraded when a positive bias is applied to the back-gate.**

I. Introduction

Mismatch in MOSFET transistors plays a crucial role in circuit design [1]. With the scaling down of analog technologies driven by low power application, mismatch origin and modelling have been widely discussed. However, in some specific cases, such as junctionless transistors [2] or mesa-isolated devices, the presence of a parasitic transistor makes a straightforward Vt matching study incomplete. In this context, we discuss a methodology to properly assess the device mismatch and compare main and parasitic transistor performances in our SOI mesa-isolated pMOSFETs.

II. Device description & methodology

SOI pMOS are defined for 2.5V applications such as sensing with channel thickness $t_{si} = 23nm$, burried oxide thickness $t_{box} = 25nm$ and SiO2-Polysilicon gate stack with EOT=6nm. Channel is undoped or doped (8e17at/cm^3, 1.5e18 at/cm^3) to allow multi Vt offer. Due to the mesa isolation, the gate stack covers the complete silicon film, including the edge as shown by TEM cross section on Fig. 1. It was shown in [3] that there are two distinct conduction regimes, one at the edges and one at the center. Thus, the entire device can be modeled as two transistors in parallel. Measurements consisted of I_d-V_g curves in linear regime (V_d=50mV) for three ground plane biases (V_b=-2.5V, 0V, 5V). We measure the V_t standard deviation of pairs of matched transistors $\sigma_{\Delta V_t}$(layout view on Fig. 1.B). Overall devices widths (W_{drawn}) and lengths (L) range from 0.2µm to 25µm.

III. Results and discussion

The edge transistor resulting from the mesa-isolation creates a hump in the I_d-V_g curve (Fig. 2.a), highlighted in the g_m/I_d curve where the highest peak comes from the edge transistor. The edge transistor is always present but not necessarily visible, as demonstrated by the single peak on gm/Id in the undoped channel case (Fig2.b). This stems from the different scaling of each transistor V_t with channel doping and back-gate bias (Fig. 2.b and 2.c). Having identified this issue, it is clear that proper care must be taken in the V_t extraction before getting to mismatch. The most straightforward methods such as extrapolation in the linear region or constant current at $10^{-7}W/L$ do not discriminate between the different regimes. V_t can be that of the edge transistor, of the center, or a mix of both depending on the geometry. The ratio method however [4], applied separately to each peak in the g_m/I_d curves (Fig 2) would be a suitable solution. Instead of the ratio method, in order to cover mismatch in the complete subthreshold regime, we chose to extract V_t at a constant current threshold for several points per decade. At low extraction current, V_t is that of the edge transistor and conversely, extracting at higher currents provides the center transistor V_t. For each threshold current value, we get the corresponding $\sigma_{\Delta V_t}$, leading to Fig. 3. Two plateaus are visible, corresponding to edge and center transistors. At low extraction currents, the two devices W_{drawn} =1µm and W_{drawn} = 25µm have similar $\sigma_{\Delta V_t}$ as expected of the edge transistor, whose dimensions do not scale with the drawn width. At higher currents, there is a x5 difference in $\sigma_{\Delta V_t}$, corresponding to a $1/\sqrt{WL}$ scaling (Pelgrom's law) as expected from a planar SOI transistor. We can get their respective iAvt considering the appropriate $\sqrt{WL}$ ratio. In [3], TCAD simulations showed that the edge conduction regime extends to about 50nm on each side. Therefore, the edge transistor width is the sum of the silicon channel thickness and the 50nm extension on both sides: $W_{edge} = 2(t_{si} + 50) = 150nm$ (Fig. 1). Complementarily, the center transistor width is $W_{center}=W_{drawn}-(W_{edge}+2t_{si})$. With the appropriate width and $\sigma_{\Delta V_t}$ (Fig. 3), the resulting Pelgrom plot in figure 4 shows a linear variation of $\sigma_{\Delta V_t}$ for both contributions. The straightforward plot with no separate normalization and extraction $10^{-7}W/L$ is also shown for comparison (green squares). The slopes are almost identical for the two devices: same matching performance is achieved (Avt =6mV.µm) for edge and center transistors. We further expand this approach to study the impact of channel doping on center and edge transistor mismatch. Same Avt increase is observed with channel doping for both top and edge transistors, (Fig 5). Finally, we address the back-bias effect on the mismatch for different doping channel. Figure 6 displays $\sigma_{\Delta V_t}$ for three different back-biases (V_b=-2.5V, 0V, 5V). At V_b=-2.5V, $\sigma_{\Delta V_t}$ is constant on the entire current threshold range, indicating that a single transistor is measured instead of two at 0V. Thus, the apparent decrease at low extraction currents is due to a change in conduction regime. On the other hand, at V_b=+5V the two different regimes are maintained and the mismatch of both transistors increases. The increase is much higher in the case of the center transistor, hence the "reverse staircase" shape compared to V_b=0V. This increase in variability for positive back-biases holds true for other dimensions, resulting in the Pelgrom plot figure 7.

IV. Conclusion

We measured matching structures of different dimensions to assess the V_t-matching of pMOS on SOI devices. Because of mesa isolation, a parasitic edge transistor is present. The edge transistor V_t-matching is identical to that of the top transistor with an Avt of 6mV.µm. The impact of channel doping and back bias were investigated. The back bias produced dramatic increase in the V_t-matching with a larger response for the center transistor.

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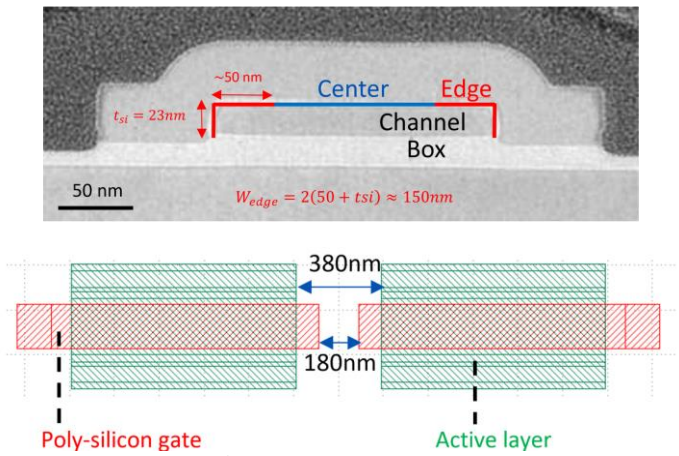

Figure 1: A) TEM view of the transistor in the width direction. B) Layout view of a pair of matched transistors

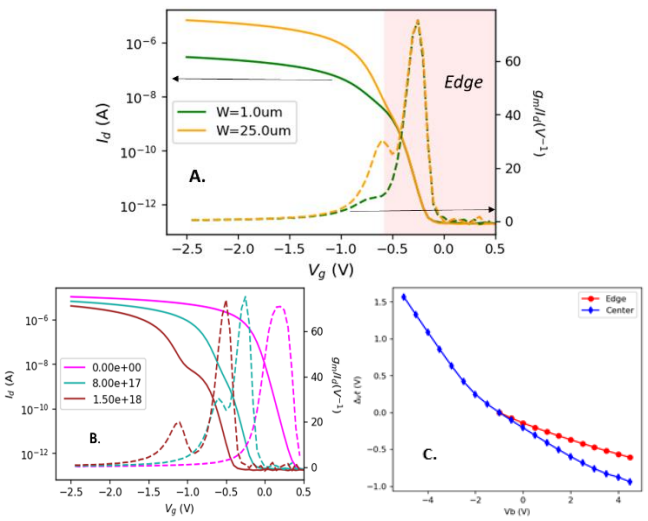

Figure 2: A) Impact of the edge transistor or I_d-V_g and g_m/I_d curves. B) g_m/I_d for different channel doping. C) Dependence of V_t to backgate-bias for both transistors (8e17 atoms/cm^3)

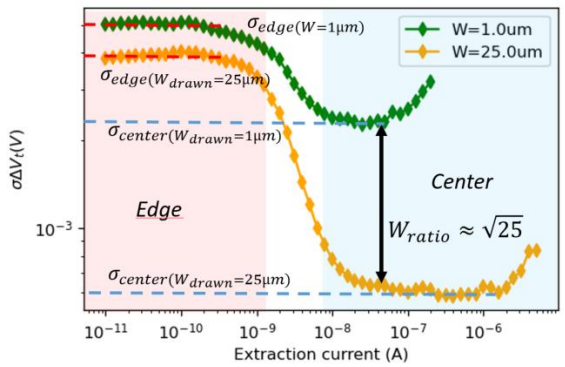

Figure 3: $\sigma_{\Delta V_t}$ as a function of the current threshold chosen for Vt extraction. Doped channel (8e17at.cm²), V_b=0V, L=10µm

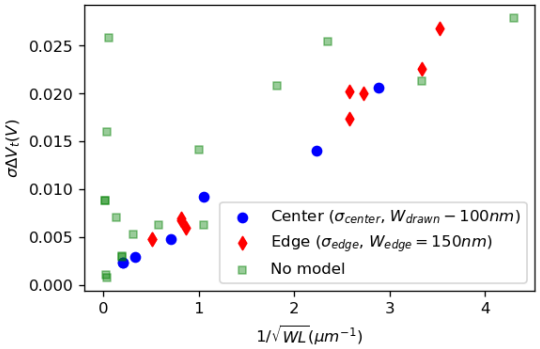

Figure 4: Pelgrom plot with separation of center and edge transistors. Normalized by 150nm for the edge and $W_{drawn} - 100nm$ for the center. (8e17 atoms/cm^3), V_b=0V

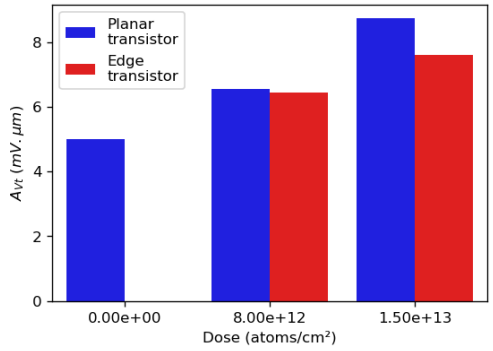

Figure 5: Avt for edge and top transistors at different doping level

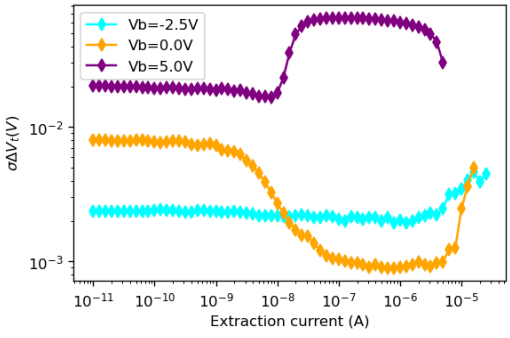

Figure 6: $\sigma_{\Delta V_t}$ as a function of the current threshold chosen for V_t extraction. W=25µm, L=10, Doped channel (8e17 at/cm^3)

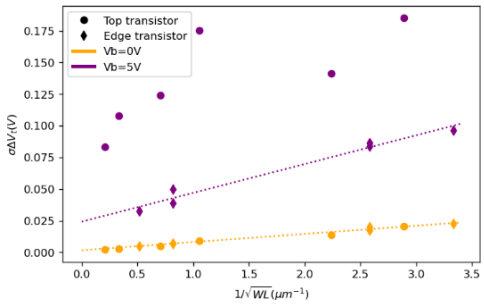

Figure 7: Pelgrom plot with separation of center and edge transistors for V_b=0Vand V_b=5V. 8e17 atoms/cm^3 devices

Analog Behavior of Forksheet at High Temperatures

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***Abstract* - This work presents the analog behavior of n-type forksheets from room to 150ºC with channel lengths of 26 and 70 nm. These devices present a Zero Temperature-Coefficient (ZTC) point for gate voltage around 0,59 V (V_{ZTC}) in saturation region. The threshold voltage variation with temperature (dV_T/dT) is around -0,5mV/ºC due to the Fermi level decrease. The DIBL increase with temperature but it is kept lower than 51mV/V in the studied temperature range. The transconductance and output conductance decrease (mainly due the mobility degradation) which results in an intrinsic voltage gain around 36 dB, showing a slight change (±2dB) in the studied temperature range. The maximum unit gain frequency was estimated around 3.87 GHz in strong inversion regime. The results show that the forksheet can also be used for analog applications at high temperature, in addition to the already known savings in footprint area compared to nanosheet technology.**

Keywords – Forksheet, Analog Parameters, High Temperature.

I. Introduction

The continuous downsizing of CMOS technology and the need to improve device performance have motivated the evolution of transistor structures from FinFETs to nanosheets [1-3]. However, with the search for a smaller footprint area in the integrated circuit, devices that integrate n and p-type transistors in the same structure have attracted the attention of the scientific community. Keeping it in mind, the complementary FETs (CFETs) [4] and forksheet [5] structures have been studied. CFET are obtained by stacking n and p-type nanosheets on top of each other, while in the forksheets the n and p-type transistor are separated by a lateral dielectric wall [6].

Complementary to the study presented in [7, 8] where the basic forksheet parameters were studied, this work focuses on analyzing the potential of forksheets for analog applications at high temperatures.

II. Device Characteristics

The forksheets were fabricated in imec/Belgiun with the details shown in [7, 8]. The forksheet schematic structure and TEM image can be seen in Fig.1. The devices used in this work are n-types with silicon thickness of H_{FS} = 7nm, silicon width of W_{FS} = 23 nm, $W_{eff} \cong$ 212 nm (2.W_{FS} + H_{FS})x4, layout gate length of L_G = 26 and 70 nm. These devices were submitted at 25ºC, 100ºC and 150ºC. The gate stack is based on HfO_2 (high-k) and TiAl (eWF layers) with EOT ≅ 1.1 nm. Only for an estimation of the unit gain frequency (f_T), it was used a p-type forksheet with large dimensions with L_G = 250 nm and W_{eff} = 31200 nm.

III. Electrical Characterization and Results

The electrical characterization of forksheet was performed using the Semiconductor Parameter Analyzer B1500 [9]. Fig. 2 shows the drain current (I_D) as a function of gate voltage (V_{GS}) in saturation region showed in linear and logarithm scale from room up to 150ºC. It is possible to observed the presence of Zero-Temperature Coefficient point (ZTC) where V_{ZTC} (V_{GS} at ZTC point) is around 0,59 V in saturation region (V_{DS}=700mV). The presence of ZTC is good for analog application. For many analog circuit applications, it is desirable to bias the devices at a point in a circuit where the voltage/current show a very little or no variation with temperature, i.e. in ZTC point. The presence of ZTC is related to the competition between the decrease of threshold voltage (V_T) and the degradation of carrier mobility (μ) when the temperature increase. For $V_{GS} < V_{ZTC}$ the V_T is the dominant factor on I_D value and for $V_{GS} > V_{ZTC}$, the μ is dominant. It is worth noting that not all devices present ZTC point. For example, the Junction-Less Transistors did not present ZTC point due to the very high series resistance, which strongly degrades the I_D and the degradation caused by temperature is not enough to overcome the increase in I_D caused by the V_T decrease, and as a consequence no ZTC is reached.

Fig.3 shows the V_T and DIBL (Drain Induced Barrier Lowering) as a function of temperature for forksheet with L_G of 26 and 70 nm. The dV_T/dT on the n-type forksheet is around -0,5mV/ºC, due to the Fermi level decrease, which is also the value observed for these devices observed from room down to 4 K [10]. The DIBL increase with the temperature but it is still low in the studied temperature range (DIBL is 51 mV/V in the worst case).

The subthreshold swing (SS) as a function of temperature (T) is shown in Fig.4. For both analyzed channel lengths, the experimental SS satisfactorily follows the ideal theoretical trends, increasing from ~62 mV at 25ºC to ~97 mV/dec at 150ºC in saturation regime. The maximum transconductance (gm_{MAX}) in linear region and the saturation transconductance (gm_{SAT} at V_{GT} = 200 mV) as a function of temperature for two channel lengths are shown in Fig.5. Both gm decrease with temperature due to the μ degradation as expected. The ratio between the gm(26nm)/gm(70nm) is lower than 2,7 (70/26) due to the fact that the effective channel length is higher than the gate layout related to the gate last process.

The forksheet transistor efficiency (gm/I_D) for different temperatures and two channel lengths is presented in Fig. 6. In weak inversion ($I_D < 10^{-8}$) the gm/I_D is inversely proportional to SS shown in Fig.4, which explain the reason for the decrement of the transistor efficient with the temperature. No relevant difference is observed for both channel lengths.

The output conduction (g_D) and Early voltage (V_{EA}) as a function of temperature for two channel lengths is shown in Fig.7. The extraction of these parameters was done at V_{DS} = 700mV and V_{GT} = 200 mV from I_D x V_{DS} curve, which is very noisy and may introduce some additional errors.

The Intrinsic voltage gain (A_V) as a function of temperature for two channel lengths is obtained (A_V=20.log($gm_{SAT}/g_{D,SAT}$)) and presented in Fig.8. For L_G=70nm the A_V is higher than L_G=26 nm due to the higher V_{EA}. The A_V variation with the temperature is not higher than ±2dB in the studied temperature range.

The unit gain frequency (f_T) as a function of drain current was estimated using a large pFET forksheet devices (L_G=250nm and W_{eff}=42800 nm) and $f_T \cong gm_{SAT}/(2.\pi.Cgg)$, where Cgg is the gate capacitance. The maximum f_T value got is 3.87 GHz at I_D=429μA (strong inversion). The f_T value may be slightly overestimated thanks to the lower Cgg value due to the high series resistance in the capacitance extraction.

The results show that in addition to the known savings in footprint area of forksheet compared to nanosheet technology (which is estimated to be around 20% lower area for logic circuit and 30% for SRAM [5]), the forksheet devices can also be used for analog applications from room to 150ºC.

IV. Conclusions

This work presents the analog behavior of forksheets from room to 150ºC. N-type forksheets with channel lengths of 26

and 70 nm were analyzed. These devices present a Zero Temperature-Coefficient point for a gate voltage around 0,59V in saturation region. The threshold voltage variation with temperature (dV_T/dT) is around -0,5mV/ºC which is the typical value for fully depleted multigate devices. Similar results for dV_T/dT were also observed in the literature for forksheet at low temperatures. The DIBL increase with temperature but it is kept low (< 50mV/V) in the studied temperature range. For both analyzed channel lengths, the experimental SS satisfactorily follows the ideal theoretical trends, increasing from ~62 mV at 25ºC to ~97 mV/dec at 150ºC in saturation regime. The transconductance and output conductance decrease due to the mobility degradation with the temperature increase. The intrinsic voltage gain of 36 dB was obtained and a slight change of ±2dB is obtained from 25ºC to 150ºC. The results show that the forksheet can also be used for analog applications in the studied temperature range, in addition to the known savings in footprint area compared to nanosheet technology.

ACKNOWLEDGMENT

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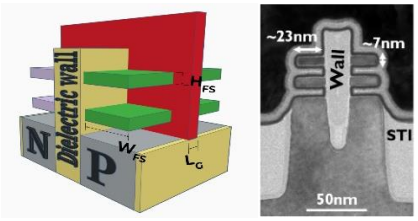

(a) (b)

Fig.1– Forksheet: (a) Schematic view and (b) TEM image perpendicular to the gate channel [7].

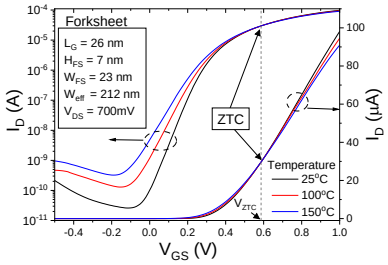

Fig.2 – Drain current as a function of gate voltage for different temperatures

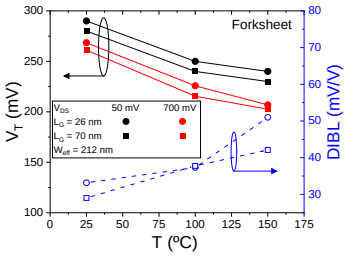

Fig. 3 – Threshold voltage and Drain-Induced-Barrier-Lowering as a function of temperature for two channel lengths.

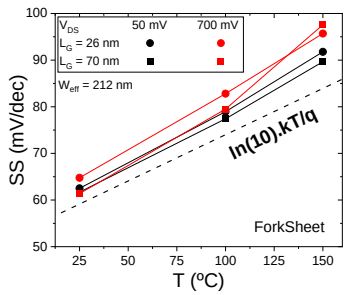

Fig. 4 – Subthreshold swing as a function of temperature for two channel lengths.

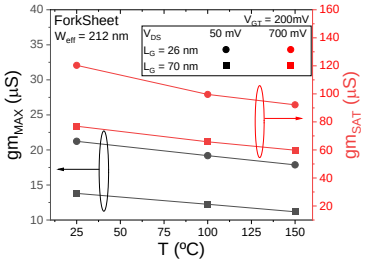

Fig. 5 – Transconductance in linear (maximum point) and saturation region (at V_{DS} = 700mV and V_{GT} =200mV) as a function of temperature for two channel lengths.

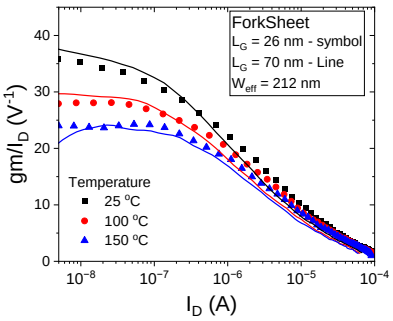

Fig. 6 – Transistor efficiency for different temperature and two channel lengths.

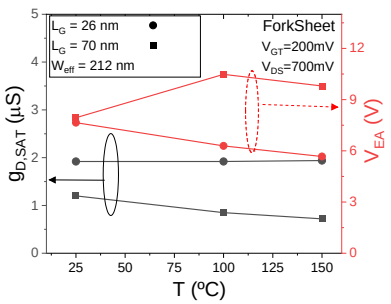

Fig. 7 – Output conduction and Early voltage as a function of temperature for two channel lengths.

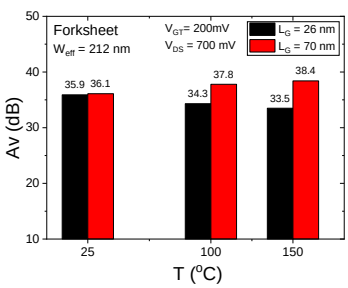

Fig. 8 – Intrinsic voltage gains as a function of temperature for two channel lengths.

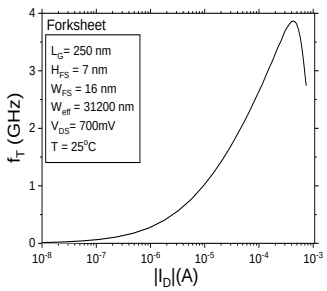

Fig.9 – Unit gain frequency as a function of drain current obtained from a large pFET forksheet dimension

Investigation of DC and Low Frequency Noise Parameters of Junctionless GAA Si VNW pMOSFETs in the Temperature Range from 80 K to 340 K

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In this article, junctionless vertical nanowire (JL VNW) Gate-all-around (GAA) silicon field-effect transistors (FETs) manufactured at imec have been studied, in a wide range of temperature from 340 K down to 80 K, by performing direct current (DC) and low-frequency noise (LFN) measurements. The aim of this experimental study is to investigate the temperature dependence of the extracted DC parameters (low field mobility (μ_0), threshold voltage (V_{th}), access resistance (R_{access}), subthreshold slope (SS) etc.), and LFN parameters (flicker (1/f) noise level, volume trap density N_{it}, etc.), for the studied devices in order to evaluate their performance. The investigated devices are silicon NWs with a diameter of ~18 nm and a length of ~56 nm, which have been epitaxially grown on Silicon-on-Insulator (SOI) substrate. They are B-doped, JL and asymmetric ($R_{Drain} \neq R_{Source}$) devices, more fabrication details can be found in [1]. Two different devices were tested, devices #1 have 20 by 20 NWs in parallel while devices #2 have 30 by 40 NWs resulting in total 400 NWs and 1200 NWs for device #1 and #2 respectively. The measurements were made in ohmic regime with a drain-source bias of $|V_{DS}|$ = 50 mV, in forward and reverse (F/R) operation mode. The experimental set-up and the parameters extraction methodology are described in [2,3]. According to the figures 1.a and 1.b (device #2, $|I_{D,(F/R)}|$ *vs.* $-V_G$ curves) an increase of leakage current in forward operation mode is observed, which may testify that, it suffers from the GIDL effect [4], due to the high doping concentration of the drain and/or the S/D asymmetry. From figure 1.c, a decrease in $|I_{D,ON}|$ for lower temperature (T), may be observed and no zero-temperature coefficient (ZTC) point was observed in the investigated temperature range. However, a better SS was perceived for lower temperatures until T = 120 K as illustrated in figure 2.a. In figure 2.b, Vth is negatively shifted with a slope of about -1.3 mV/K. A significant degradation of the low field mobility is noticed as the temperature decreases. It may be suggested that scattering by surface oxide charges may be the dominating mechanism causing μ_0 degradation as can be observed in figure 2.c, since the evolution of the extracted μ_0 is proportional to the temperature [5]. It is important to note that a decrease in the extracted R_{access}, when the temperature decreases was also observed for both devices, see Figure 2.c (right). On the other hand, the LFN measurements reveal an increase in the input referred noise power spectral density (PSD) as the temperature decreases for the same $|V_{ov}|$, ($|V_G$-Vth|) as illustrated in figure 3.a. Figure 3.b shows the 1/f noise level *vs.* $|V_{ov}|$ for device #1. For T = 300 K, the dominant noise contributions are the correlated carrier number and mobility fluctuations mechanism (CMF + CNF), and the R_{access} noise contribution at high $|V_{ov}|$ values, (no impact of the S/D asymmetry was observed on the LFN). For T = 150 K and 80 K only CMF + CNF was observed, which may be related to the decreasing of the R_{access}. A correlation was fond between mobility μ_0 degradation and the estimated flat-band noise level (S_{vfb}) and N_{it} increasing as exposed in figure 3.c. This correlation suggests an impact of the charge oxide traps on both 1/f noise level and low filed mobility through remote Coulomb scattering.

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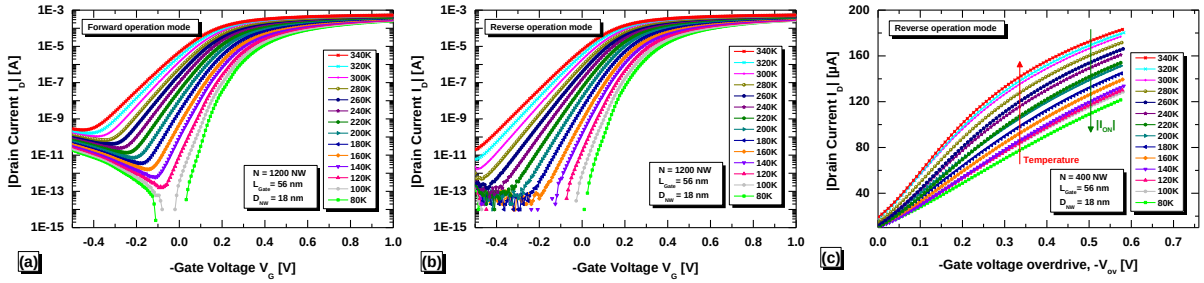

Figure 1: Absolute drain current $|I_D|$ *vs.* - applied gate voltage in forward (a) and reverse (b) operation mode (in log scale) as a function of temperature for device #2 (1200 NWs). (c) Absolute drain current $|I_D|$ (in linear scale) *vs.* absolute gate voltage overdrive $|V_G\text{-Vth}|$ for device #1 (400 NWs) as a function of temperature.

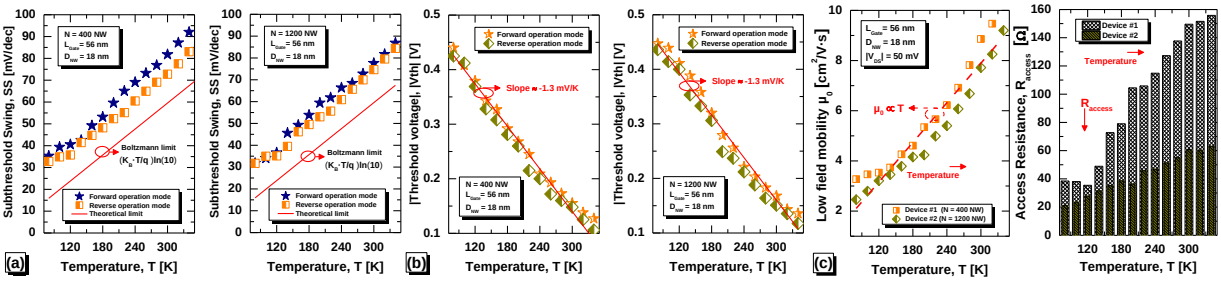

Figure 2: (a) SS as a function of temperature for device #1 (left) and device #2 (right). (b) Threshold voltage Vth as a function of temperature with $|V_{DS}|$= 50 mV. (c) Extracted low field mobility parameter μ_0 (left) and access resistance $R_{accesss}$ (right) *vs.* temperature for the studied devices.

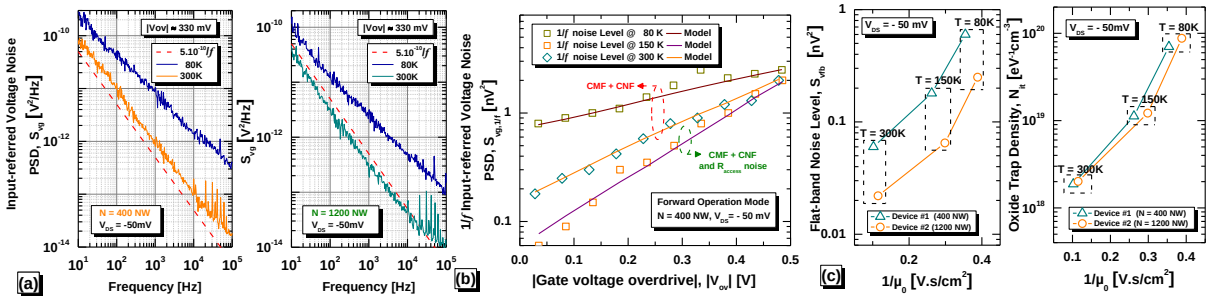

Figure 3: (a) typical 1/f input-referred voltage noise PSD S_{vg} *vs.* frequency for different temperatures at $|V_{ov}| \approx$ 0.330 V and V_{DS} = -50mV for device #1 and #2. (b) Input-referred 1/f noise level *vs.* the gate voltage overdrive (V_{ov}), for temperatures T=300 K, 150 K and 80 K for device #1. (c) Estimated flat-band noise levels (left) and N_{it} (right) *vs.* the inverse of the extracted low field mobility for T = 300 K, 150 K and 80 K for device #1 and #2.

Novel Y-function methodology parameter estimation from weak to strong inversion operation

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Considering the expressions of the drain current and of the transconductance in ohmic operation regime [1], and of the general assumed extrinsic effective mobility [2,3]:

$$I_D = \frac{W}{L}\mu_{eff}Q_iV_{DS} \quad (1)\,; \quad g_m = \frac{WV_{DS}}{L}\frac{C_{ox}C_i}{C_{ox}+C_d+C_{it}+C_i}\frac{\partial(\mu_{eff}Q_i)}{\partial Q_i} \quad (2); \quad \mu_{eff} = \frac{\mu_0}{1+\theta_1(Q_i/C_{ox})+\theta_2(Q_i/C_{ox})^2} \quad (3)$$

the expression of the Y-function may be derived as:

$$Y = \frac{I_D}{\sqrt{g_m}} = \frac{\sqrt{G_MV_{DS}}}{\sqrt{1-\theta_2(Q_i/C_{ox})^2}}\sqrt{\left(\frac{SS}{\ln 10}+\frac{Q_i}{C_{ox}}\right)\frac{Q_i}{C_{ox}}} \quad (4)$$

where $G_M = W\mu_0C_{ox}/L$ [2]; W and L the effective width and length of the channel; μ_{eff} the extrinsic effective mobility; μ_0 the low field mobility; θ_1 and θ_2 the first and second mobility attenuation factors; Q_i the inversion charge density; V_{DS} the drain to source voltage; C_{ox}, C_d, C_{it} and C_i are the gate, depletion, interface state and inversion charge capacitances per unit or area and SS the subthreshold swing. Assuming that $C_i \ll C_{ox}+C_d+C_{it}$ in weak inversion and $C_i \gg C_{ox}+C_d+C_{it}$ in strong inversion with $C_i = qQ_i/(k_BT)$ (k_BT/q being the thermal voltage) [1] the Q_i/C_{ox} may be evaluated: in weak inversion as: $Q_i/C_{ox} = Y^2/G_MV_{DS}\,SS/\ln 10$ (5) and in strong inversion as $Q_i/C_{ox} = Y/\sqrt{G_MV_{DS}+\theta_2Y^2}$ (6). Without any approximation, from weak to strong inversion the ratio Q_i/C_{ox} may be expressed as: $(G_MV_{DS}+\theta_2Y^2)\left(\frac{Q_i}{C_{ox}}\right)^2 + G_MV_{DS}\frac{SS}{\ln 10}\frac{Q_i}{C_{ox}} - Y^2 = 0$ (7).

The G_M and θ_2 parameters were extracted using criteria of [3] and the subthreshold swing SS may by determined from I-V curves in the subthreshold zone. Consequently, the Q_i/C_{ox} ratio may be easily evaluated from weak to strong inversion operation by solving the second-degree equation of (7) (Figure 1). Further, the drain current may be evaluated using (1), having θ_1 estimated using [3] and the transconductance using (2) or $g_m = {I_D}^2/Y^2$, where Y is modeled using (3). Very good agreement between the experimental I_D and the g_m models of (1), respectively (2) may be observed for devices for different technologies (Figure 2 and 3), even at 80 K operation (Figure 3).

The advantage of this new methodology is that no capacitance measurements or mathematical formulation as Lambert W function or Kubo-Greenwood modeling approach are necessary [4,5]. Moreover, only four parameters are needed to be estimated: three extracted in strong inversion (G_M, θ_2 and θ_1) and one estimated in the subthreshold zone (SS). The inversion charge over the gate capacitance ratio is estimated using its dependency on the Y-function described in (7). Finally, a compact Y-function methodology may be proposed, providing accurate and physical electrical parameters extraction and allowing to model the transfer characteristics behaviour from weak to strong inversion operation regime if the drain current may be expressed as in (1) and the extrinsic effective mobility as in (3).

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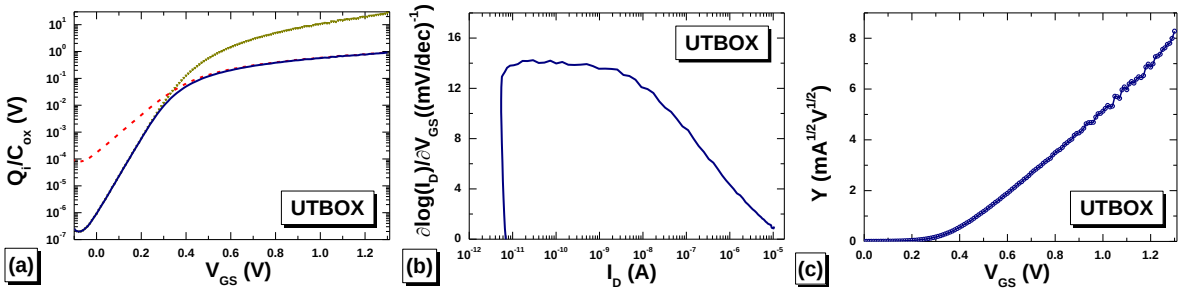

Figure 1: (a) Q_i/C_{ox} versus the applied gate voltage estimated from (5) (short-dot line), from (6) (short dash line) and from (7) (full line). (b) $\partial\log(I_D)/\partial V_{GS}$ permitting the estimation of the SS parameter. (c) very good agreement between the experimental Y-function and model of (4). UTBOX n-channel device: L / W = 120 nm / 1 µm, EOT of 2.6 nm, after processing a BOX thickness T_{BOX} of 15 nm and a silicon film thickness T_{Si} of 16 nm.

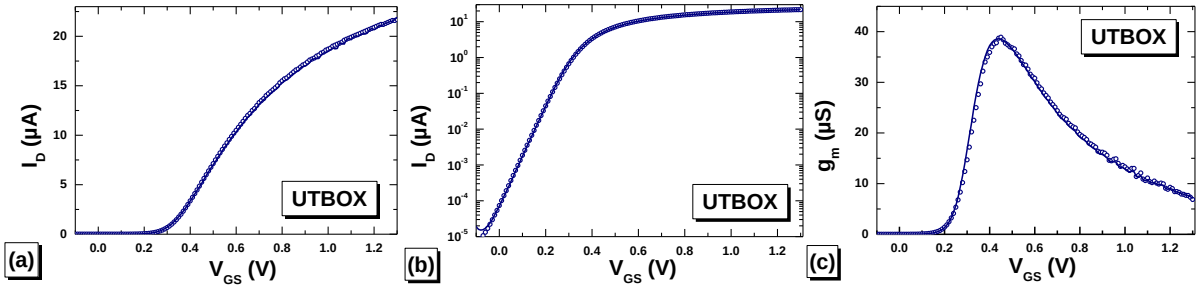

Figure 2: I_D *vs.* V_{GS} in linear scale (a) and log-lin scale (b); (c) g_m *vs.* V_{GS}; Good agreement between the experimental (symbols) and the model (full line) is observed.

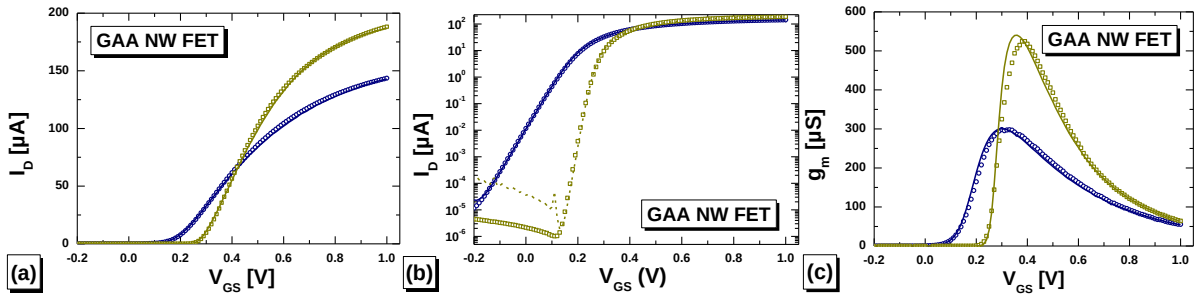

Figure 3: I_D *vs.* V_{GS} in linear scale (a) and log-lin scale (b); (c) g_m *vs.* V_{GS}, Good agreement between the experimental (symbols) and the model (full line) can be observed. circle points represent 300 K, square points represent 80 K temperature operation. GAA NS FET device: L / W = 100 nm / 2288 nm, EOT of 0.9 nm; vertical distance between the stacked nanosheets 7.5 nm.

The Dual-Technology FET: nMOS/pTFET in the same device

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Abstract **- This work presents for the first time the experimental results of a Dual-Technology FET (DT-FET). DT-FET is a SOI transistor capable of operating either as an n-type MOSFET (nMOS) or a p-type Tunnel-FET (pTFET), depending on the back gate bias and the source/drain bias conditions. It is an extension of the ^{BE}SOI MOSFET, with the addition of N+ at the drain or source region, which results in different physics of operation depending on back the gate bias. For a positive back gate bias the device behaves as an nMOS, while for a negative back gate bias it behaves as a pTFET. The results were compared with 2D simulations, showing that the overall trends are similar.**

Keywords – Reconfigurable Transistor, nMOS, Tunnel-FET.

I. Introduction

In recent years, the study of reconfigurable transistors has yielded many different structures and technologies [1,2]. Of particular interest to this work is the ^{BE}SOI MOSFET, patented in 2015 [3], which has a very simple fabrication process and depends only on the back gate bias to switch between an n-type or p-type device. Here, we propose a new type of reconfigurability: not only changing the type of the device, but also its main conduction mechanism. Therefore, instead of changing between nMOS or pMOS, we propose a device that switches between nMOS and pTFET. One possible application of this kind of device is to use it as an nMOS for digital circuits and as a pTFET in analog circuits where it is well-known the superior behavior due the lower output conductance presented by silicon-tunnel FETs [4].

II. Device Characteristics

Figure 1 shows the device structure profile and the top view of the fabricated device. Different from the conventional MOSFET structure, one side of the device is left intentionally undoped during the fabrication, so that the back bias may perform the electrostatic doping on it [5]. The fabricated devices have a gate stack of Aluminum, gate oxide of 10 nm, silicon film of 20 nm and buried oxide of 200 nm. On the drain side a phosphorus doping of around 10^{20}cm^{-3} was performed. The channel and the source side are kept with the natural wafer doping of Boron at 10^{15} cm^{-3}. The fabricated devices were also simulated with these same characteristics using a 2D-numerical device simulator (Sentaurus TCAD) in order to see the tendencies observed experimentally in both technology operation. To simulate the tunneling, both Trap-Assisted Tunneling (TAT) and Band to Band Tunneling (BTBT) were considered, using Hurx's model for the TAT and a non-local path for the BTBT.

III. Electrical Characterization and Results

One important remark is that, since the DT-FET is asymmetrical, the definition of drain and source is back gate bias dependent. In Figure 1, two different situations are shown in the schematic representation: if biased as an nMOS (positive back gate bias), a positive drain should be applied to the doped side; if biased as a pTFET (negative back gate bias), a negative drain voltage should be applied to the undoped side.

Figures 2 and 3 present the experimental results of the DT-FET operating as an nMOS, in linear and saturation region respectively, while Figure 4 and 5 show the simulation results, demonstrating that the overall trends are kept, although the numerical values are different, mainly due to the simulated contacts, which were considered to be ohmic, but might not be the case [6]. Besides that, the usual dependency between back gate bias and threshold voltage may be observed in these figures, as should be expected from SOI devices [7], and an average subthreshold slope of approximately 100 mV/dec was extracted.

Figures 6 and 7 show respectively the experimental normalized drain current as a function of the front gate voltage of the DT-FET operating as a pTFET in linear and saturation like region. Figures 8 and 9 present the same results for the simulated devices. Here it must be considered that the series resistance does not have direct impact on the drain current, since the overall current is dominated by the tunneling resistance. Besides that, no ambipolar current is observed both in simulation and experiments, and little variation with respect to the back gate bias is obtained.

The presented results demonstrate that this device, which has a simple fabrication process, is able to operate as nMOSFET or pTFET only changing the applied bias. Considering that this device is manufactured in silicon, with a fully compatible CMOS processing, and knowing the excellent analog potential of Si-TFETs, as a future application it can be proposed that it operates as a MOSFET for digital blocks and as a TFET for analog blocks.

IV. Conclusions

The Dual-Technology FET has been presented for the first time, with experimental results showing that it can operate as an nMOS or as a pTFET depending on the biases applied to the back gate. The experimental observations follow trends similar to those of the simulations, showing that the fabricated devices followed the expected behavior.

Acknowledgment

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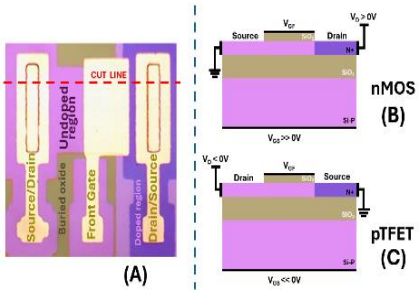

Fig.1– (A) Photo of the fabricated DT-FET (B) DT-FET device structure operating as an nMOS

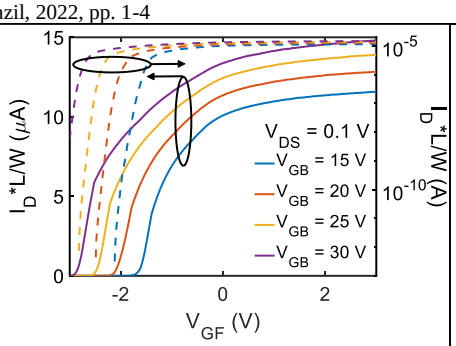

Fig. 2 – Experimental drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 0.1 V.

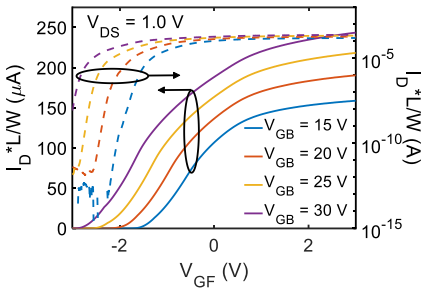

Fig. 3 – Experimental drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 1.0 V

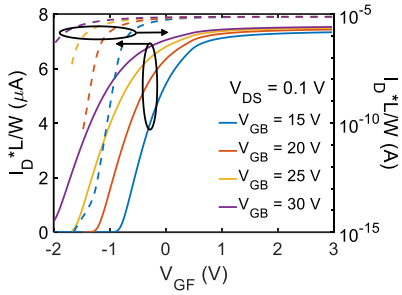

Fig. 4 – Simulated drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 0.1 V

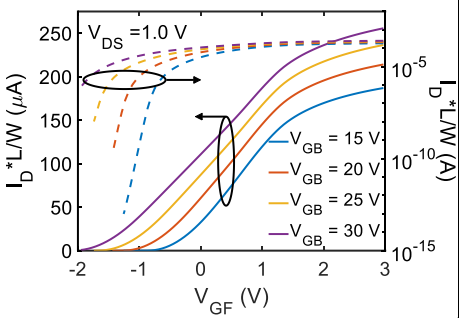

Fig. 5 – Simulated drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 1.0 V

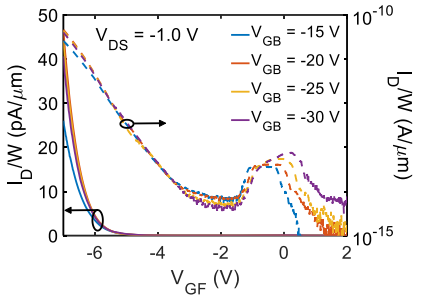

Fig. 6 – Experimental drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at 1 V

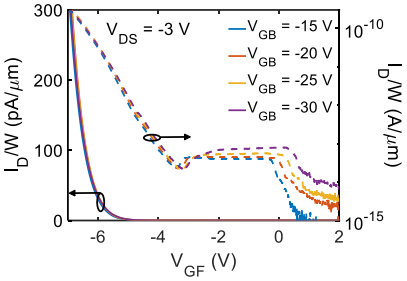

Fig. 7 – Experimental drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -3 V

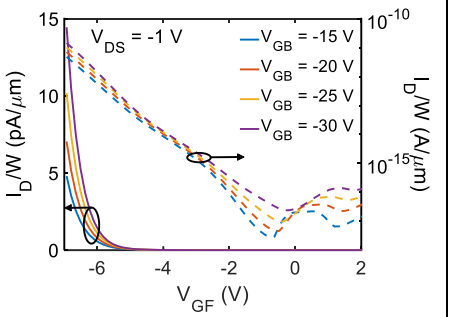

Fig. 8 – Simulated drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -1 V

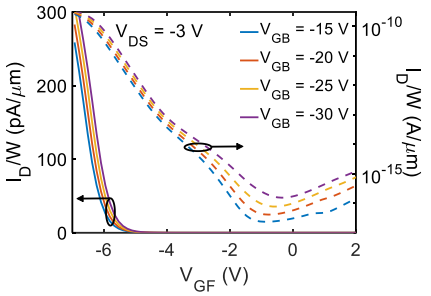

Fig. 9 – Simulated drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -3 V

TLM-based numerical extraction for CMOS-compatible N$^+$-InGaAs ohmic contacts on 200mm Si substrates

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Abstract – We report the results of a TLM-based numerical extraction methodology applied on CMOS-compatible n$^+$-InGaAs ohmic contacts integrated with dielectrics on 200mm Si substrate. We obtained state-of-the-art level ρ_c = 7,5.10^{-8} ohm.cm² for relevant contact dimensions (THz HBT for 6G). This methodology is first described and calibrated using contacts on SOI.

Introduction

As the demand for increased data rates is growing in telecommunications, 6G/sub-millimeter Wave (sub-mmW) aims to achieve the desired capacity through operation at very high frequencies (~300GHz). InP-based devices are nowadays the best-in-class devices to operate efficiently at these frequencies [1]. Achieving high performance and stable ohmic contacts using CMOS-compatible metallization is a first challenge to overcome to address HBT-InP based circuits integration on large scale silicon. To obtain 6G/sub-mmW requirements such as THz Maximum Frequency of Oscillation, values in the order of 10^{-8} ohm.cm² for the specific contact resistivity are required mainly for emitter and base contacts of the transistor [2], as HBT frequency performance is directly linked to the ohmic contacts quality. Structures with dimensions as close as possible to the common THz HBTs emitter, base and collector contact dimensions are thus necessary for accurate contact evaluation.

Device description and TLM interpretation

TLM structures with contact dimensions from 5x5µm to 0.35x0.35µm are formed on integrated $In_{0.53}Ga_{0.47}As$/InP stacks on a 200mm silicon manufacturing platform (Fig. 1). Structures were first measured following the classical TLM extraction methodology. However, interpreting the resistivity results is not straightforward as the mesa geometry of our structures is incompatible with usual TLM assumptions [3]. Indeed, as the δ distance (invariant versus contact geometry) becomes significant for low contact dimensions, the global current path within the structure geometry has to be considered, see Fig. 2. To address this issue, we directly considered our contact and mesa geometries using numerical simulation (COMSOL software). Borders of the structures are considered fully isolated and resistivity induced by the contact metal stack is ignored, as it has been evaluated to be negligible. Contact resistivity and conductivity values are respectively set to the metal/semiconductor interfaces and to the semiconductor layer.

Results and discussion

To calibrate our extraction methodology, we first used our numerical model on n-type SOI stacks (Fig. 3). Initial ρ_c and R_{sh} values for simulation were taken from TLM measurements realized on the largest available contact area (5x5µm). As Fig. 3 shows, we can correctly assess the measured current levels for larger contact dimensions with the initial ρ_c and R_{sh} values. However, for smaller ones (0.35x0.35µm), significant errors appear for low spacing distance (*d*) values, meaning that these contacts are not accurately modeled. We thus adjust the ρ_c and R_{sh} values by determining how they individually affect the fitting of the curves for the 0.35x0.35µm geometry, see Fig. 4. Values providing the best overall fit along all spacing distances (*d*) are retained and reinjected into the simulation. We found out this allows to assess a single value of ρ_c and R_{sh} for all contact geometries, as less than 3.5% error is obtained between measured and simulated current levels. Our numerical solution thus properly models the contact for all dimensions. Numerically extracted R_{sh} and ρ_c are then compared with classical TLM extraction. Sheet resistivity is only modified by +4% whereas ρ_c can be over-evaluated by ~50% using classical TLM extraction methodology, depending on the contact geometry (Table 1). This confirms that classical TLM interpretation is limited for scaled contact geometries as in our case. This methodology has then be used to extract the contact resistivity of CMOS-compatible Ti-based contact on n$^+$-InGaAs layers. Extraction for 0.35x0.35µm contact leads to ρ_c = 7,5.10^{-8} ohm.cm² value (Fig. 5). It is 15.3% less than the value extracted using classical TLM interpretation. Such ρ_c value on n$^+$-InGaAs is comparable to the state-of-the-art, see Table 2. This is a convincing and encouraging result for future HBT-InP emitter and collector contacts fully integrated in silicon environment, with values of 10^{-8} ohm.cm².

Conclusion – A TLM-based numerical extraction has been proposed to properly extract the sheet resistance and contact resistivity of CMOS-compatible ohmic contacts on n-InGaAs layers. This refinement allows to reduce errors by 15.3% compared to classical TLM extraction for such scaled contacts. The obtained ρ_c value is compatible with 6G THz applications and comparable to the state-of-the-art.

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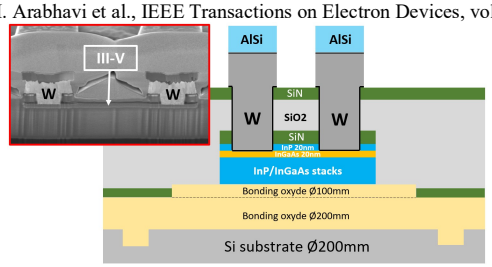

Fig. 1: Schematic view and FIB-STEM picture of the technology stack embedded in dielectrics. The Ti/TiN/W/Ti/AlSi metallization is deposited to contact the n+-InGaAs layer, doped $N_d = 5.10^{19}$ cm^{-3}.

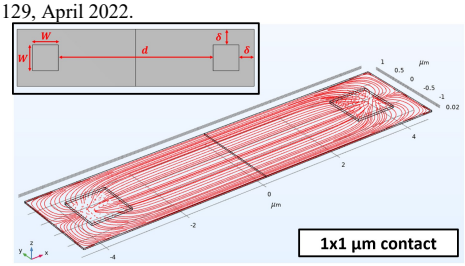

Fig. 2: Reproduction of measured ohmic contact-based structures for TLM extraction of electrical parameters with a COMSOL assisted methodology. 3D current flow is adequately assessed regarding mesa geometry (large δ distance).

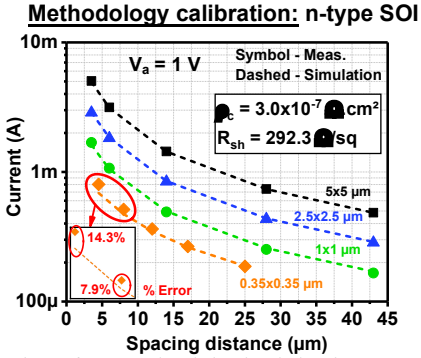

Fig. 3: Comparison of measured and simulated electric currents according to geometries. Smaller contacts (relevant for our application) are not accurately modeled using ρ_c and R_{sh} from 5x5µm contacts obtained from classical TLM analysis.

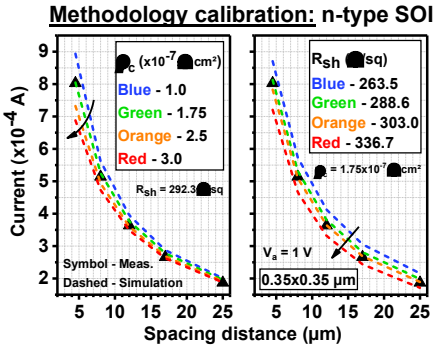

Fig. 4: Impact of ρ_c (left) and R_{sh} (right) modification on the simulated electric current curves. ρ_c affects the offset and the slope of the curves for small *d* values (left). Modifying R_{sh} (right) applies a global offset to the curves.

Methodology calibration: n-type SOI

Contact geometry (µm)	Classical TLM ρ_c extraction (10^{-7} ohm.cm²)	Simulation ρ_c extraction (10^{-7} ohm.cm²)	% Error
5 x 5	3.04	1.75	- 42.4 %
2.5 x 2.5	3.60		-51.4 %
1 x 1	2.15		- 18.4 %
0.35 x 0.35	1.84		- 4.9 %

Table 1: ρ_c extraction difference between classical TLM methodology and simulation based on n-doped SOI stacks. Large contact extraction leads to ~50% error. Our simulation allows to fit all results with only one ρ_c value.

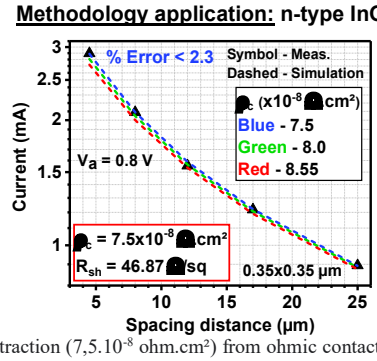

Fig. 5: ρ_c extraction (7,5.10^{-8} ohm.cm²) from ohmic contacts on n-type InGaAs in CMOS-compatible integration using our methodology. Standard TLM extraction yields 8,85.10^{-8} ohm.cm² (15.3% error).

	This work	[4]	[5]	[6]	[7]	[8]
n-InGaAs doping level (10^{19} cm^{-3})	**5.0**	~7.5	Not specified	3.0	1.0	1.0
Contact metal	**Ti (/TiN/W)**	Ti (/TiN/W)	W	Mo (/W)	Mo (/Ti/TiN/W)	Ti (/Pt/Au)
CMOS-compatible process integration	**Yes**	Yes	Yes	No	No	No
Substrate	**Si 200mm**	Si 200mm	Si 200mm	Si (Ø not specified)	Si (Ø not specified)	InP (Ø not specified)
Contact area for resistivity extraction	**0.35 x 0.35 µm**	0.05 x 2 µm	0.09 x 0.463 µm	/	/	25 x 30 µm
ρ_c (10^{-8} ohm.cm²)	**7.5**	72	7.51	0.8	~1.6	~2.0

⇨ used in **[9]**

Table 2: Benchmark of ohmic contacts on n-InGaAs. Our CMOS-compatible process yields values in line with state-of-the-art for THz HBT [8-9].

Effect of Al_2O_3 on the operation of SiN_X-based MIS RRAMs

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A large variety of resistive memory (RRAM) technologies are prominent. Nevertheless, a few fulfill the requirements for CMOS integration and meet the commercialization standards. SiN_X was found to exhibit competitive resistance switching (RS) properties and attractive SiN_X-based RRAM devices have been recently demonstrated [1-3] utilizing a metal-insulator-semiconductor structure comprising 7nm LPCVD SiN_X (x = 1.27) on heavily doped n^{++} Si ($N_d = 1\times10^{20}$ /cm^3) and 30nm Cu acting as bottom (BE) and top electrode (TE) respectively. Al_2O_3 has been used in the past as a buffer layer in RRAMs to improve the RS and the cycle-to-cycle variations [4]. In this context, we investigated the effect of inserting a thin Alumina layer between the top electrode and SiN. A reference sample without the Al_2O_3 was prepared for the shake of comparison (Figure 1). The 3nm Al_2O_3 layer was deposited by MEMS ALD. The TE was covered by a 30nm Pt to prevent oxidation.

Figure 2a presents I-V curves measured for different compliance currents (I_{CC}). The SET and RESET voltages were statistically analyzed in Figure 2b and statistical analyses revealed that the addition of Al_2O_3 slightly reduced the HRS variability. Nevertheless, LRS variability increased. The mean SET voltage of the Al_2O_3/SiN_X sample is 0.9V higher than the reference, which equals the voltage drop on the Al_2O_3 when 5V is applied to the TE according to simulation results. This means that the addition of Al_2O_3 on SiN_X does not alter its operation as a switching material. Multiple SET/RESET cycles were performed using voltage sweeps (I_{CC} 100μA). The current at high resistance (HRS) and low resistance (LRS) states is monitored at 0.5V. The Al_2O_3/SiN_X can endure significantly lower number of cycles compared to the reference sample which is probably be attributed to the higher SET/RESET voltages used for Al_2O_3/SiN_X sample. The memory window (LRS/HRS) evolution with the number of cycling voltage is shown in Figure 2c. Specifically, it begins at 10^4 and is stabilized to 10^5. This behavior has been previously observed in reference samples [6] and is attributed to the gradual reduction of the length of the raptured conductive filaments during cycling.

Moreover, impedance spectroscopy measurements were performed for pristine and cycled devices, i.e., after the SET/RESET sweeps using different SET I_{CC}. The Nyquist plots for Al_2O_3/SiN_X devices at LRS form a semicircle (Figure 3a), indicative of an equivalent circuit consisting of a resistor (R_p) and a capacitor (C_p) in parallel and a resistor in series (R_s). Physically, R_p and C_p correspond to the resistance of the conductive paths formed during SET and the capacitance of the remaining insulating (no-switched) material region, respectively. The dielectric constant (ε') was also extracted (Figure 3b) for pristine samples, and it was found to be significantly higher (~7.7) than the reference sample (~5.5),

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which is expected due to the addition of the 3nm Al_2O_3. Furthermore, the AC conductance (σ') was calculated (Figure 3c) by subtracting the dc part from the measurements and it becomes clear that σ' varies as ~f^s. The values of exponent s range from 1.59 to 1.67 and denote that during SET conduction in SiN_X is mainly governed by trap-to-trap tunneling mechanisms (s is close to 2) [5].

Acknowledgements

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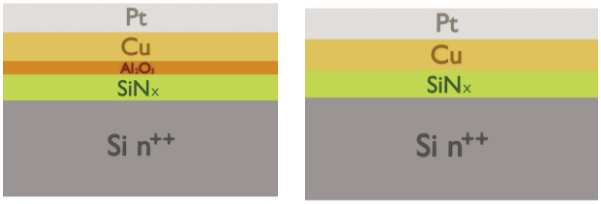

Figure 1 Fabricated Al_2O_3/SiN_X and SiN_X (reference) samples.

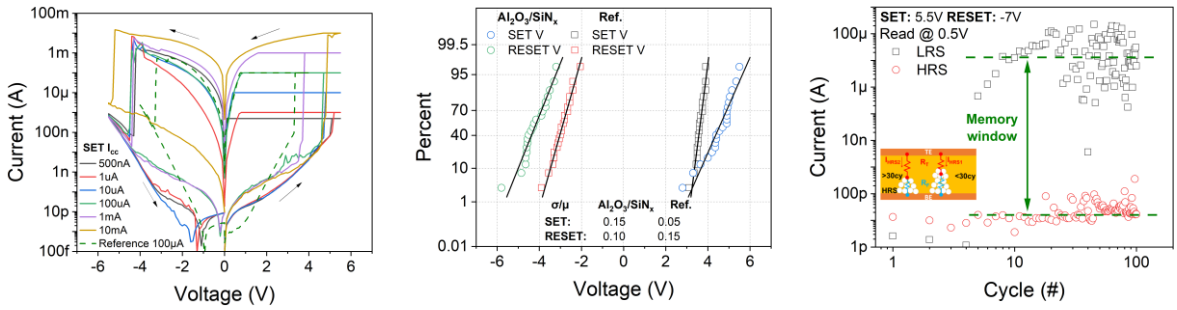

Figure 2 a) I-V sweeps with different I_{CC}, b) SET/RESET voltage statistics and c) HRS/LRS at 0.5V.

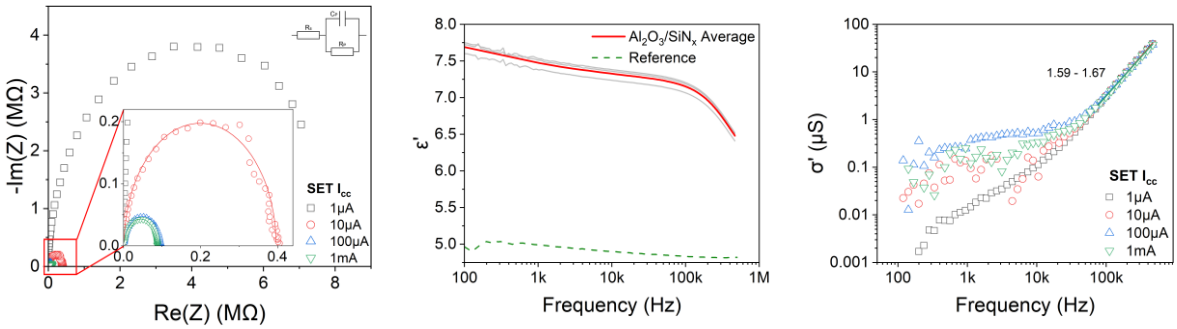

Figure 3 a) Nyquist plots of Al_2O_3/SiN_X devices SET, b) dielectric constant of pristine sample and c) AC conductance of Al_2O_3 sample.

Amorphous TeO_2 as P-type Oxide Semiconductor for BEOL Devices

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Back-end-of-line devices need amorphous dopable bipolar oxide semiconductors. However, there are no practical p-type oxides, they are layered, require high processing temperatures or ineffective due to self-compensation by native defects. TeO_2 is a glass. Our simulations find that amorphous (a-) TeO_2 is chemically ordered, can be degenerately doped p-type, does not self-compensate and uses low-cost processable materials.

There is presently an intensive search for practical back-end-of-line (BEOL) oxides that can be doped n- or p-type. There are many n-type oxides like InGaZn oxide. However, there are no low-cost p-type oxides with hole mobility. Compounds like $CuAlO_2$ do not favor disorder due to their layered structure [1], $ZnRh_2O_4$ uses high-temperature refractory metals [2], while SnO is p-type but its 0.7eV indirect gap causes large leakage currents [3]. Ternary oxides like $SnTa_2O_6$ have wider gaps [4] but their dopability is limited by intrinsic oxygen vacancies V_O^{2+}, a key factor that is rarely tested [5-8]. β-TeO_2 has a high hole mobility (3000 cm^2/V.s, calculated [9]), ~300 cm^2/V.s experimental [10] due to s-like upper valence band [9-11].

We show here that a-TeO_2 can be doped p-type and can be structurally disordered without suffering V_O^{2+} self-compensation, making it the first viable p-type oxide semiconductor.

The electronic structures of rutile and layered (β- or α-) phases of TeO_2 are calculated by density functional theory (GGA) and with HSE hybrid functional bandgap corrections. Electron affinity (EA) and ionization potential (IP) energies below the vacuum level are found using a supercell with a 15Å vacuum spacing. Defect compensation is calculated from the defect formation energy ΔH_q [5]

$$\Delta H_q(\mu,E_f) = E_q - E_H + q\Delta E_f + \Sigma n_\alpha \mu_\alpha$$

as a function of the host total energy E_H, the defect charge (q), and the Fermi energy (E_f) with respect to the valence band edge, n_α is the number of atoms of element α and μ_α is the chemical potential of α.

The amorphous oxide is studied by ab-initio molecular dynamics (AIMD) for a 120-atom crystalline cell heated to 2000K for 4ps, cooled to 300K, and then relaxed at 300K for 5 ns. Doped oxide, not yet studied, is modeled by substituting two As_{Te} sites, to avoid needing spin polarisation.

β-TeO_2 is a quasi-layer compound, with an orthorhombic structure, stabilized from its rutile-TeO_2 phase by a 0.2 eV per formula unit (fu), Fig. 1, Table 1. Fig. 2(a,b) compares the HSE band structures of β-TeO_2 and rutile-TeO_2. The EA and IP of β-TeO_2 for bulk cells are found to be 3.16 eV and 6.45 eV respectively, consistent with previous studies [10,12]. There is a direct 3.3 eV bandgap at Γ and a shallow Te s-like valence band maximum (Fig. 3), giving a small hole mass and high theoretical hole mobility.

Fig. 4(a) shows a structural model of a-TeO_2 by AIMD. Locally, it resembles β-TeO_2, with 4-fold Te sites and 2-fold O sites. The O bridges are not always grouped in bridge pairs. Fig. 5(b) shows the radial distribution function (RDF) of this disordered TeO_2. The first neighbor peak due to heteropolar Te-O bonds occurs at 1.96 Å, with second neighbor peaks at 2.8Å due to O-O bonds and 3.8Å peak from Te-Te bonds, as earlier [12]. There are no first-neighbor homopolar bonds. Thus, although O and Te are both chalcogens, their sizable electronegativity difference strongly favors heteropolar bonding. Hence, the chemical ordering of a-TeO_2 is quite similar to that in β-TeO_2, while allowing structural disorder to occur. Previously a notable type of disorder was due to varying the number of long (non-covalent) Te-O bonds [13]

Fig 5 shows the calculated defect formation energies ΔH of the oxygen vacancy V_O for O-poor and O-rich β-TeO_2, where V_O is the principal compensating defect. We see that ΔH of V_O^{2+} crosses the 0 eV axis below the valence band edge, ie. ΔH is positive within the gap, so these defects are endothermic and they do not cause self-compensation. Other defects, the interstitials I_O, I_{Te} and vacancy V_{Te} are less problem.

Fig. 6 compares the calculated absolute EA and IP values to the estimated doping limits of oxides [6]. The IP of β-TeO_2 is close to the doping limit for p-type oxides. However, these limits apply best if the compensating defect is a V_O defect in an ionic lattice. TeO_2 is a mainly covalent Te-O-Te network, and this pushes the lower doping limit downwards somewhat.

Although self-compensation is the key aspect, it is critical to test the actual dopability of a-TeO_2 directly by creating substitutional dopant sites like As_{Te} or Sb_{Te}. In Fig. 7, we insert two As atoms into a AIMD supercell and find that E_F lies at the valence band edge of a-TeO_2. Thus, TeO_2:As differs from Ga_2O_3 with its deep acceptors. This is a useful test. Zavabeti [10] studied the undoped oxide experimentally but not the doped oxide. These still need a check experimentally. It is interesting that TeO_2 is unusual that it can be shallow doped p-type by N of the O site, in contrast to ZnO or Ga_2O_3.

We have calculated the key factors needed to test defect self-compensation and disorder tolerance for a-TeO_2 to be classed as a viable p-type semiconductor for BEOL devices.

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Table 1.: Comparison of rutile, α-, and β-TeO_2.

	rutile-TeO_2	α-TeO_2	β-TeO_2
Symmetry	$P4_2/mnm$	$P4_12_12$	P_{bca}
Crystal system	Rutile	Distorted rutile	Ortho-rhombic
E_{form} eV/f.u	-1.27	-1.49	-1.49
Gap (eV) (HSE)	0.72	2.65	3.29
IP (eV) (HSE)	6.09	7.31	6.45
EA (eV) (HSE)	5.37	4.66	3.16
Band gap	indirect	indirect	direct

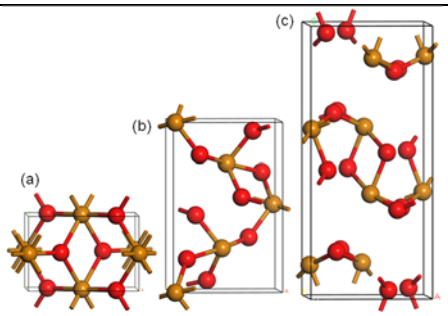

Fig. 1(a) rutile TeO_2, (b) α-TeO_2, (c) β-TeO_2

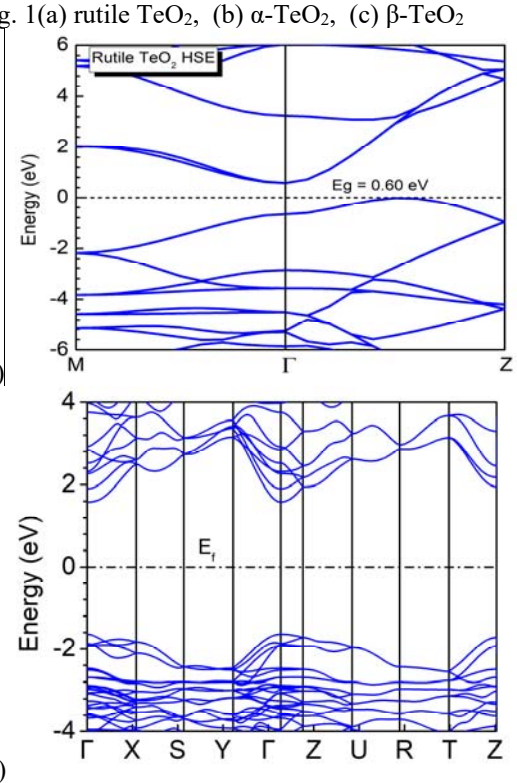

Fig. 2. HSE Bands of (a) rutile TeO_2, (b) β-TeO_2.

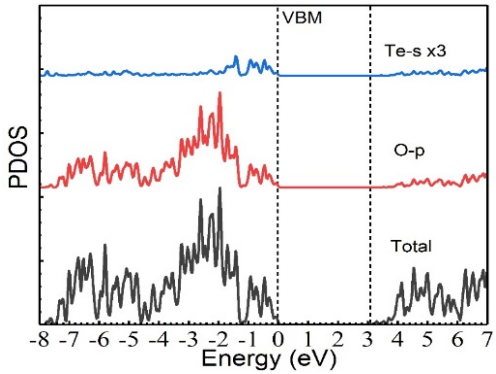

Fig. 3. Partial density of states (PDOS) of β-TeO_2

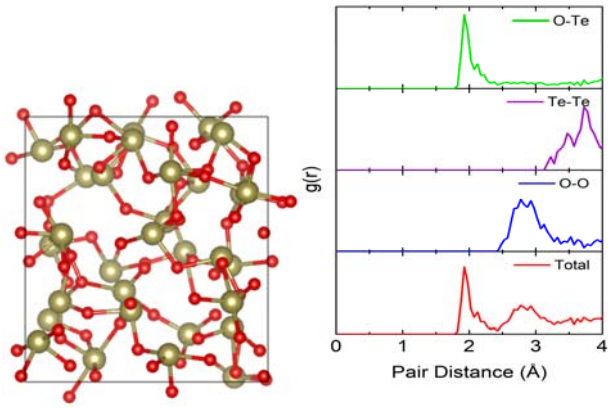

Fig 4(a). Structural model of a-TeO_2 by AIMD and (b) calculated RDF of this model.

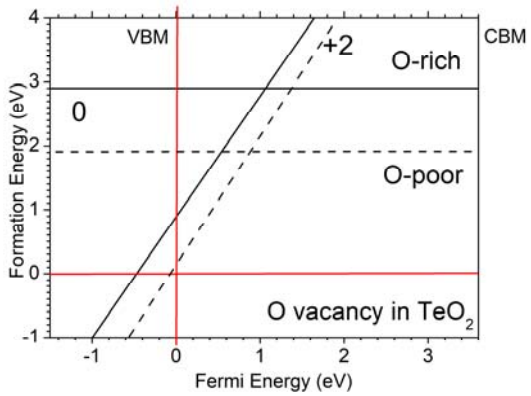

Fig 5 Defect formation energy vs.Fermi energy, for V_O self-compensation for O-rich and O-poor β-TeO_2.

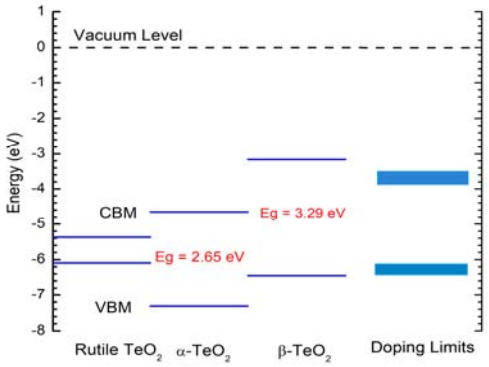

Fig. 6: Band-edge energies of TeO_2 phase vs. vacuum level, compared to approximate doping-limit energies [7].

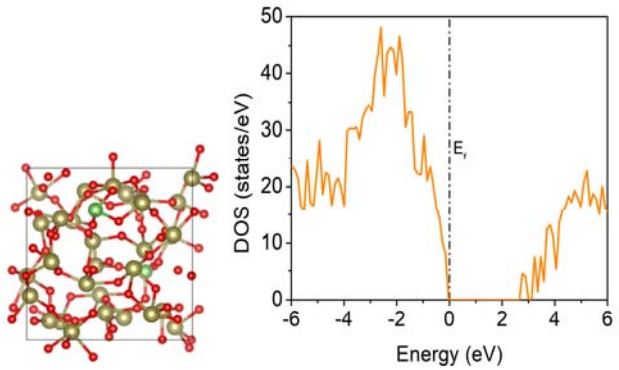

Fig. 7(a) network structure and (b) DOS with two As_{Te} acceptor sites, showing shallow doping in a-TeO_2 with E_F at the valence band edge.

Trap Characterization in Substrates with Buried SiGe Layers for RF

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When it comes to radio-frequency (RF) applications, an SOI substrate requires low propagation losses and harmonic distortion at microwave frequencies, and this necessitates a high effective resistivity. However, fixed charges present at the BOX/semiconductor bottom interface attract free carriers toward the interface, lowering the effective resistivity of the substrate. This is referred to as the parasitic surface conduction (PSC) that undermines the efficacy of employing a High-Resistivity (HR) substrate. One efficient way to reduce free carriers near the Si surface and conserve the high resistivity of the substrate is to take advantage of a large density of interface traps (D_{it}) at the SiO_2/Si interface. High interface trapping states lead to deep Fermi level pinning in the band gap, so that the free carrier concentrations remain low, ensuring a state of high resistivity. In our work, an epitaxial SiGe layer is inserted under the BOX between SiO_2 and Si. A SiO_2/SiGe interface tends to have higher D_{it} values than SiO_2/Si, attributed to the formation of Ge-O bonds in the interfacial layer [1]. Consequently, it would be valuable to investigate D_{it} and the effective resistivity (ρ_{eff}) in different buried SiGe substrates.

Fig. 1 shows schematic cross-sections of a SiGe MOS capacitor (a) and a coplanar waveguide (CPW) transmission line structure (b). Here, R_s is the series resistance of the Si substrate. C_{ox} is the capacitance of the dielectric stack. C_c and G_c are the corrected capacitance and conductance. G_p and C_p are the parallel equivalent conductance and capacitance, respectively, corresponding to the SiO_2/SiGe interface. SiGe/Si is assumed to be interface trap-free. Table I lists the compositions of five buried SiGe substrates and the related thickness of different SiGe.

Using the series resistance correction model (SRC) proposed by Nicollian [2] presented in Fig. 1 (a), Fig. 2 (a) shows C_c-V from 1 kHz to 1 MHz. One can see the flatband voltages shift towards negative values with increased frequencies, preventing a conventional flatband extraction. This horizontal frequency-dependent shift can be explained with the effective pinned Fermi level by high D_{it} at the interface SiO_2/SiGe [3]. The "bump" arises within the inversion region, where the increase in capacitance under positive bias with decreasing frequency is largely mitigated. This could also be attributed to a high interface trap density effectively stabilizing the Fermi level [4]. The extraction of average substrate p-type doping concentration, N_A (= 1.10×10^{15} cm^{-3}) is here based on the slope of the linear part of the $(1/C_c)^2$ curve versus the applied voltage in the inset [5], corresponding to 14 Ω·cm for all SiGe samples. Fig.2 (b) shows the G_p/ω - f curves. The peak positions of the G_p/ω (f) curves shift to high voltage values with decreased frequency due to the presence of interface trap states. Therefore, we obtain the interface trap response for a gate voltage range from -3.5 to 6 V.

Fig. 3 (a) shows the D_{it} ($\Delta E = E_T - E_v$) profiles of samples 3 and 4, the trap energy states distributed in the band from 0.3 to 0.5 eV above the valence band (D_{it} values of all the samples listed in Table I). In Fig. 3 (b), the ρ_{eff} of sample 3 with a higher D_{it} value appears flatter and higher compared to sample 4 in the range of -15 to 15 V. Differing from samples 3 and 4, the ρ_{eff} value of standard Si (15-20 Ω·cm) are lower and dependent on gate bias. The boost of ρ_{eff} is attributed to the higher D_{it} at SiO_2/SiGe compared to SiO_2/Si. The simulation for sample 3 aligns with its characterization, which can then be used to model high resistivity buried SiGe substrate. To give insight into the potential of SiGe solution in enabling high-quality RF performance, buried SiGe (500 Ω·cm) high resistivity Si substrate (2 kΩ·cm) is employed in the TCAD simulation, as seen in Table I. It presents a high ρ_{eff} above 2 kΩ·cm being bias independent due to the sufficient compensation provided by the interface traps.

Summarizing, the efficiency of the buried SiGe substrate has been characterized. Both small signal measurements and simulations demonstrated that high D_{it} extracted from the conductance method at an SiO_2/SiGe interface can neutralize the free carriers coming from bulk, thus overcoming the PSC effect and ensuring a state of high resistivity. High resistivity buried SiGe substrate emerges as a promising candidate for RF SOI integration. At the same time, a buried SiGe layer can be a useful layer being able to induce tensile strain in the channel of an SOI MOSFET if both the SOI and BOX layers are extremely thin (FD-SOI), thereby boosting transistor mobility [6].

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TABLE I SUMMARY OF PARAMETERS OF SUBSTRATES

Sample number	SiGe thickness (Å)	%Ge	D_{it} ($eV^{-1}cm^{-2}$)	ρ_{eff} (Ω·cm) @ 2 GHz @ 0 V
1	90	20	2.2×10^{12}	44.6
2	130	20	2.2×10^{12}	44.8
3	700	20	2.5×10^{12}	44.8
4	60	40	1.8×10^{12}	40.6
5	110	30	8.0×10^{11}	41.5
Standard Si	-	-	2.5×10^{11} [2]	21.5
500 Ωcm SiGe/HR Si (TCAD)	1100	20	2.2×10^{12}	5213

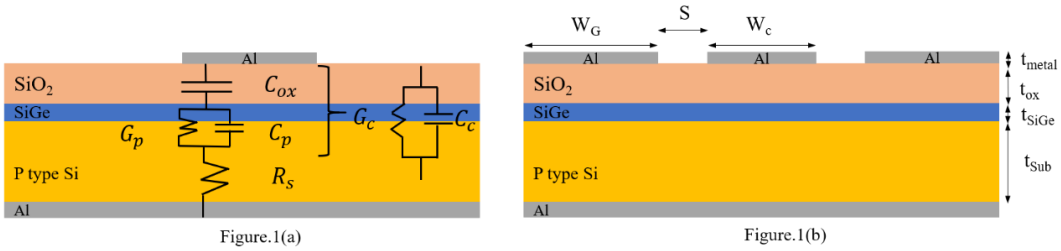

Figure.1(a) Figure.1(b)

Figure 1. (a) The cross-section of SiGe buried capacitor. (b) The cross-section of a CPW line on top of SiGe buried substrate (Parameters: t_{metal} = 1 um, t_{ox} = 200 nm, W_c = 26 µm, W_G = 208 µm, and S = 12 µm).

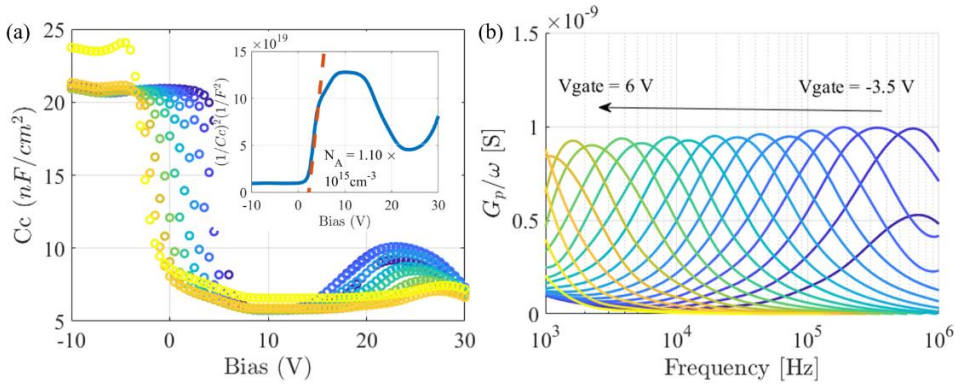

Figure 2. (a) C_c – V and (b) G_p/ω - f from 1 kHz to 1 MHz for sample 2. The inset in (a) corresponds to N_A extraction.

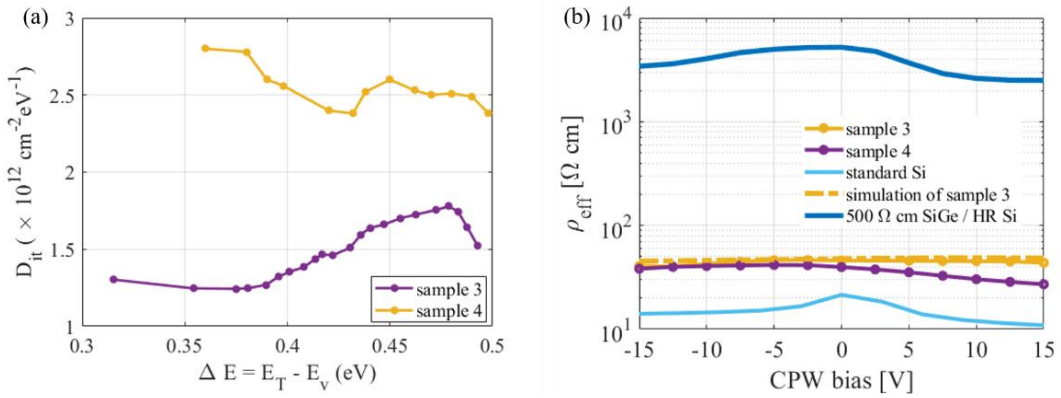

Figure 3. (a) D_{it} ($\Delta E = E_T - E_v$) profile of samples 3 and 4, respectively. (b) CPW line effective resistivity of samples 3, 4, standard Si, and 500 Ω cm SiGe/HR Si extracted at 2 GHz as a function of applied bias from -15 to 15 V.

Substrate Crosstalk Characterization for optimized Isolation in FDSOI

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The continued large-scale integration of CMOS technologies has enabled complex system on chip (SoC) applications. These SoC systems often integrate a logic circuits (aggressor) along with sensitive analog and RF circuit blocks (victim). The dynamic signal switching of logic block couples through the substrate and impact the performance or functionality of the sensitive analog/RF block. The fundamentals of crosstalk between noise source and victim are well discussed in the literature. The approach for crosstalk reduction is often driven in terms of substrate resistivity (i.e., either very low (~1 mΩ.cm) [1] or high (>1 kΩ.cm)) and introduction of conductive layers in SOI system [2],[3]. It has been demonstrated that triple wells in bulk CMOS can be equal or better in isolation compared to SOI [4]. However, for mixed mode CMOS circuits, the choice of specialized substrate is not trivial. This work consolidates the solutions of crosstalk reduction in commercial SOI resistivity substrate (~1 – 100 Ω.cm) by investigating design-based solutions in fully depleted SOI (FDSOI) technology. This crosstalk study evaluates the isolation in term of SOI vs. bulk, junction impact, lateral resistance, and noise shunting elements (guard-rings). A novel guard-ring scheme deploying the combination of resistive and capacitive elements for a superior isolation is demonstrated.

The test structures are designed using 22nm FDSOI process in ground signal ground layout as shown in Fig. 1. The parameter S_{21} from 2-port S-Parameters measurement is used as a metric to evaluate crosstalk isolation. At first the reference is established for devices in bulk and SOI separated by STI as shown in Fig. 2. The STI oxide inhibit the surface coupling component between aggressor and victim which is evident with increased spacing. SOI devices exhibit significant lower crosstalk (~ -100 dB) at the lower frequency regime due to BOX indicated by the slope of 40 dB/dec until the inflection point of 3 GHz. The increase of lateral resistance can also be achieved by deploying pn junctions. In addition, a shunting path for noise signal in the form of guard-rings further reduces the crosstalk. Fig. 3 shows that for bulk devices, the introduction of a single and double pn-junction reduces the crosstalk by ~55 dB and ~80 dB at 40 MHz respectively. The bulk test structure with double junction shows 40 dB/dec slope beyond 200 MHz indicating a similar isolation to SOI integration. On the other hand, SOI devices with the resistive guard-ring show minor dependency of the pn-junctions on crosstalk magnitude and slope. For superior isolation over the wide frequency range the combine resistive and capacitive guarding can be combined as shown in Fig. 1(b). Fig. 4. demonstrate improved crosstalk isolation for mixed guard-ring at higher frequencies (> 1 GHz) while keeping the total guard ring area the same. The benefit of adding capacitive guarding to the existing resistive guarding translated to 8 dB at 10 GHz for double pn-junction. The SOI devices with MxCap guard-ring design exhibit overall the best crosstalk isolation followed up by the resistive guard-ring. The improved isolation of MxCap guard-ring compared to bulk device with resistive guard-ring is clearly observed for frequencies > 400KHz.

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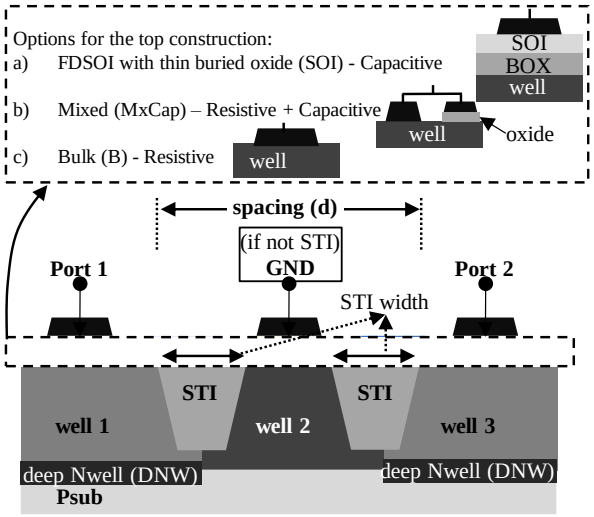

Fig. 1. Cross-section of the 2-port experimental test structures. Port 1 and port 2 can be regarded as noise source and victim devices. The center optional terminal "GND" acts as a noise-shunt or guard-ring. The design variables are: type of well (n/p-type), device type (SOI or bulk), type of guard-ring, spacing between noise source and victim.

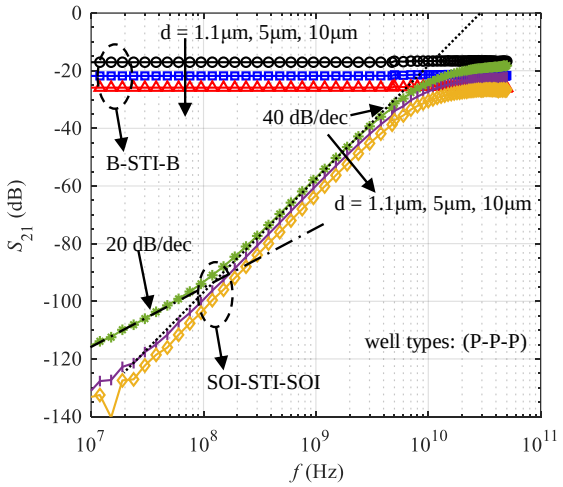

Fig. 2. S_{21} magnitude (crosstalk) vs. frequency for the structure with STI separating aggressor and victim devices. The well type are mentioned as: (well 1 – well 2 – well 3). The top construction scheme follows the convention i.e. (device type Port 1 – guard-ring – device type Port 2).

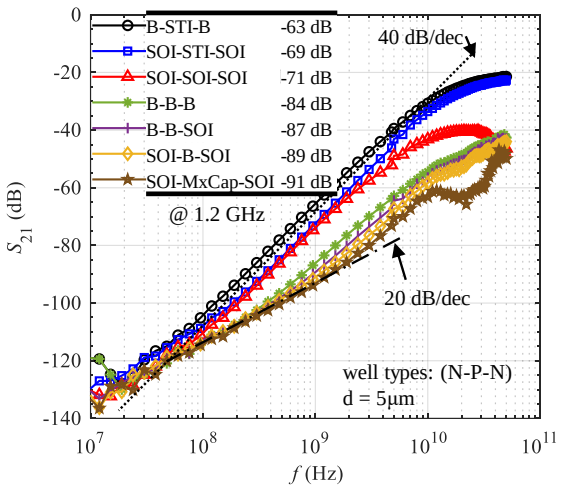

Fig. 3. Crosstalk measurement of bulk and SOI devices with resistive type guard-ring having spacing of 1.1 µm.

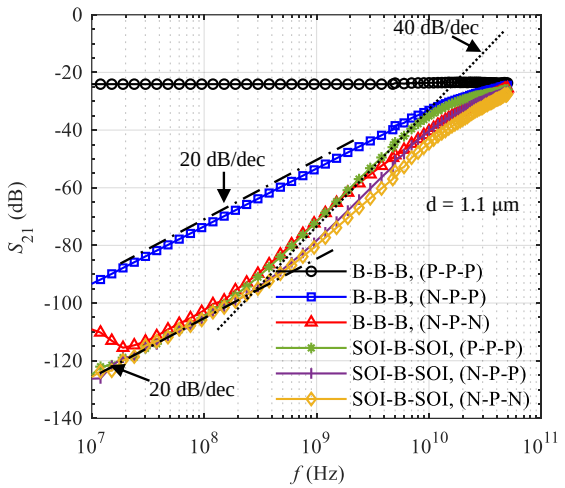

Fig. 4. Comparison of crosstalk for all top contruction of bulk and SOI type agressor/victim. The magnitude of S_{21} at the frequency of 1.2 GHz is listed in the legend table.

GaN-on-GaN PiN Diode Performance at Cryogenic Temperatures

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Spacecraft based electronic systems require cryogenic temperatures for their operation. Hence, it is of paramount importance to design power electronics systems that can operate efficiently under these conditions. A recent review [1] of power semiconductor devices at cryogenic temperatures included SiC Schottky diodes and GaN High Electron Mobility Transistors (HEMT), but no studies have been reported on the electrical behavior of GaN based diodes. This paper presents a comprehensive study of the performance of GaN-on-GaN PiN diodes at cryogenic temperatures.

A schematic cross-section of a fabricated GaN-on-GaN PiN diode is depicted in Fig. 1. The epitaxial structure comprises of 300 nm p GaN, 8 µm n^- GaN and 350 µm n^+ GaN. Multiple metal layers of Ti/Al/Ti/Au were deposited consecutively on the backside of substrate, and subsequently annealed at 825°C for 30 s in N_2 ambient to form an ohmic contact. Finally, Ni/Au metals were deposited on the p GaN and annealed at 550°C for 10 minutes in O_2 ambient to form the anode electrode. Current-voltage (I-V) measurements were recorded over the temperature range from 300 K down to a cryogenic temperature of 80 K. The forward voltage current density and on-resistance (R_{on}) curves are shown in Fig. 2. The turn-on voltage (V_{on}) is found to be 3.48±0.06 V (@ J=1 A/cm^2), while the forward voltage and on-resistance are 5.66±0.1 (@ J=100 A/cm^2), and 22.39±3.16 mΩcm^2, respectively. The temperature dependent forward I-V curves are shown in Figs. 3-4. It can be seen from the inset of Fig. 3 that V_{on} increases as temperature decreases. A similar trend can be seen for R_{on} from Fig. 5. The total on-resistance consists of the resistances of drift layer, substrate, and contact, each with a different contribution. The carrier concentration in the n^- GaN layer is extracted to be 4.55×10^{16} cm^{-3}, as shown in Fig. 6. The total current density has been estimated as the sum of separate contributions, according to the schematic in Fig. 7. The results indicate the dominance of Shockley-Read-Hall recombination [2] and its strong sensitivity to temperature. Due to the higher activation energy of Mg and Si in GaN, the physical model of incomplete ionization [3] is introduced in the modelling of the current to investigate the impurity freeze-out effect. Furthermore, the temperature dependent band gap [4] and mobility [5] models are included and will be discussed in detail in the full paper. Unlike GaN HEMTs [1], the carrier freeze-out has been observed in the GaN-on-GaN PiN diode. Further optimization and improvements of the diode model is required to explain current transport at cryogenic temperatures.

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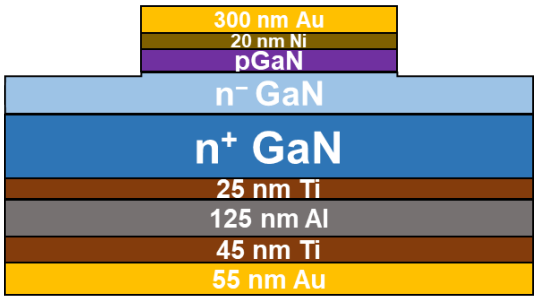

Fig. 1 Schematic cross-section of GaN-on-GaN PiN diode.

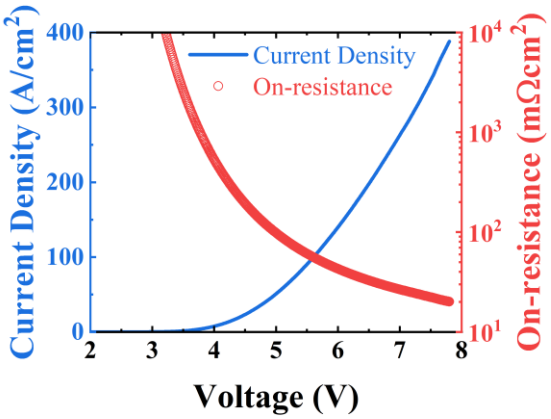

Fig. 2 Forward J-V and R_{on} vs. voltage curves.

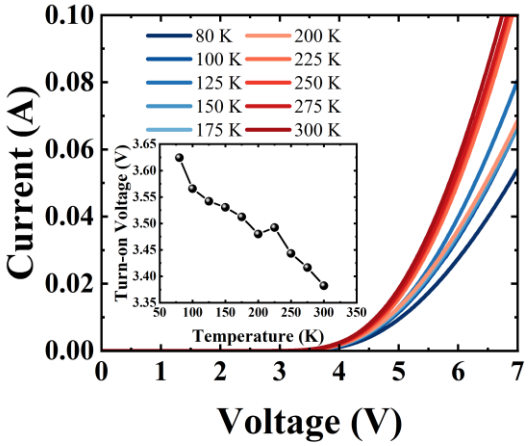

Fig. 3 Temperature dependent I-V curves on a linear scale with V_{on} vs. temperature in the inset.

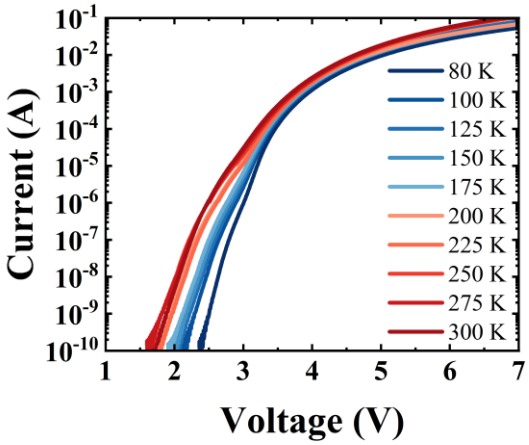

Fig. 4 Temperature-dependent I-V curves on log scale.

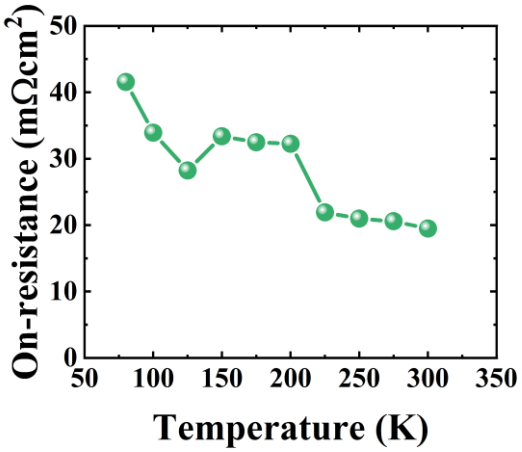

Fig. 5 On-resistance versus Temperature

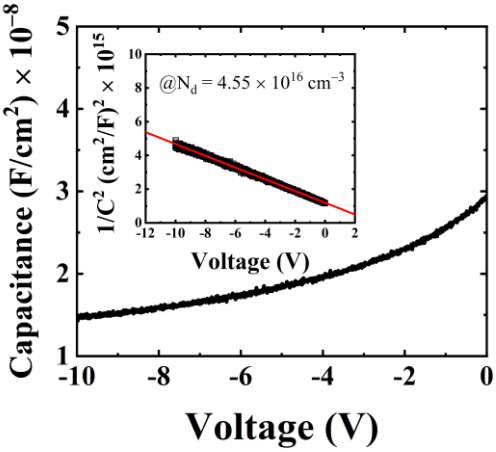

Fig. 6 C-V and $1/C^2$ vs. voltage in the inset.

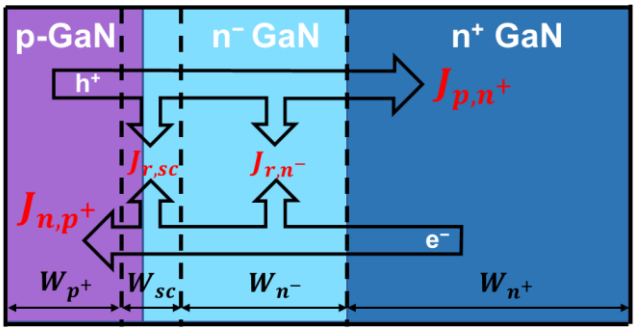

Fig. 7 The cross-section of p GaN - n^- GaN - n^+ GaN showing contribution of several current components (diffusion and recombination) considered in modelling experimental I-V curves at cryogenic temperatures.

Low-frequency Noise in Polysilicon Source-Gated Thin-Film Transistor

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In thin-film field-effect transistors (TFET) that aim at high-voltage operation for e.g. large-area display or analog applications, by overlapping the gate with a Schottky source contact, a new type of device named Source-Gated Transistor (SGT) [1] provides many advantages, such as reduced short-channel effects and high intrinsic gain [2]. Low-frequency noise (LFN) like $1/f$ noise is critical for analog circuits, has barely been studied in SGTs. Hence, in this work, $1/f$ noise of silicon-on-insulator (SOI)-based polysilicon TFETs and SGTs is investigated.

The schematic cross-section of the device is shown in Fig. 1(a) [3]. The device width, channel length (d) and source length (s) are 50, 4 and 4 µm, respectively. The polysilicon layer is 40 nm thick and n-doped. The device transfer and output curves are illustrated in Fig. 1(b) and (c) for 2 different n-type bulk doping doses. The current clearly saturates at very low drain voltage (below 1 V) and that the output impedances are considerably high, due to the pinch-off region under source that induced by the reverse biased Schottky barrier.

Fig. 2 shows drain current noise spectral densities (S_{id}) of SGT devices measured in linear operation (V_{DS} = 0.5 V). The S_{id} follows the behavior of typical $1/f^{\gamma}$ where γ is close to 1. To study the current level dependence (fig. 2b-c), the carrier number fluctuation (CNF) model ($S_{id}/(I_d^2) = (g_m/I_d)^2 \bullet S_{vfb}$) is considered [4], where g_m is the device transconductance and S_{vfb} is the flat-band voltage noise spectral density. In Fig. 3, the normalized noise spectral densities (S_{id}/I_d^2) at 10 Hz vary proportionally to $(g_m/I_d)^2$ under high I_d in both linear (V_{DS} = 0.5 V) and saturation regimes (V_{DS} = 5 V), which implies that the $1/f$ noise is mainly correlated to the CNF, while the noise under low I_d relates to the fluctuation in Schottky barrier height [5]. By swapping the source with another drain, we obtain the characteristics of a standard polysilicon TFET for comparison. In Fig. 4, the S_{id}/I_d^2 at 10 Hz of counterpart TFET device deviates from $(g_m/I_d)^2$ and varies approximately as I_d^{-1}, which suggests the carrier mobility fluctuation (CMF) dominates low-frequency noise in this case [4], while CNF is not completely ruled out.

In conclusion, the low-frequency noise of SOI-based polysilicon SGTs appears dominated by CNF in high I_d region and by Schottky barrier height fluctuation in low I_d region, while the low-frequency noise of polysilicon TFET appears mainly correlated with the CMF. Further studies are required to comprehensively investigate the LFN dependence in SGT with source length and Schottky barrier height, which are crucial parameters for SGT behaviors and optimization.

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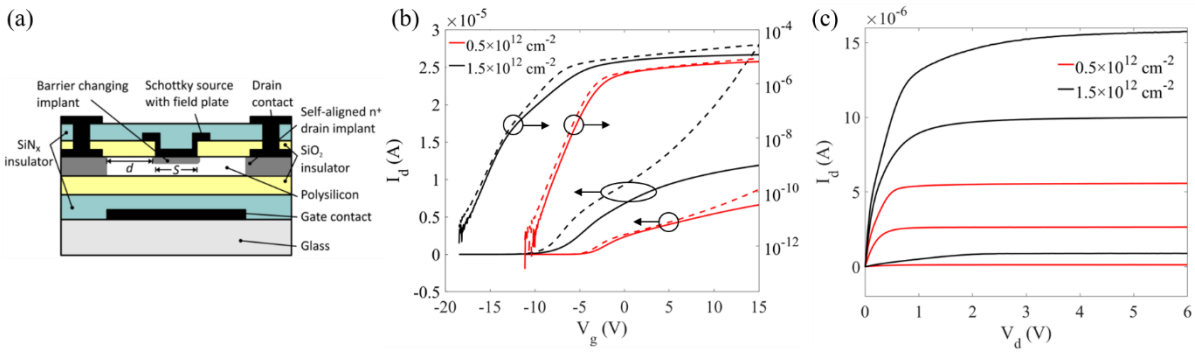

Fig.1 (a) Schematic cross-section of the SOI polysilicon SGT [4]. (b) Transfer curves for 2 different doping doses at V_{DS} = 0.5 V (solid lines) and 5 V (dashed lines). (c) Output characteristics under different gate voltages for 0.5×10^{12} and 0.5×10^{12} cm^{-2} doping doses.

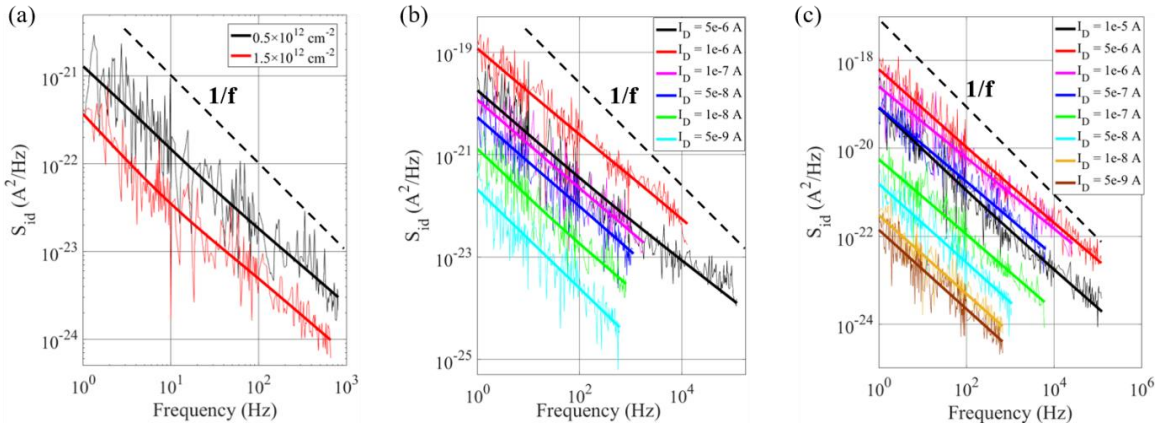

Fig.2 Current noise spectral densities (S_{id}) for the devices with (a) both doping doses at fixed drain current I_D = 10 nA, (b, c) different fixed I_D at doping doses = 0.5×10^{12} (b) and 1.5×10^{12} cm^{-2} (c) respectively. V_{DS} = 0.5 V.

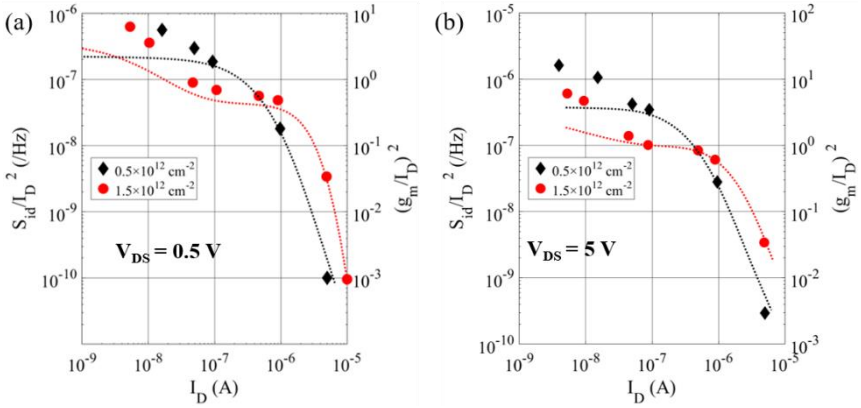

Fig.3 Normalized S_{id} / I_D^2 at 10 Hz (dots) and $(g_m/I_D)^2$ (dashed lines) as functions of I_D for SGT for the 2 different doping doses at V_{DS} = 0.5 (a) and 5 V (b).

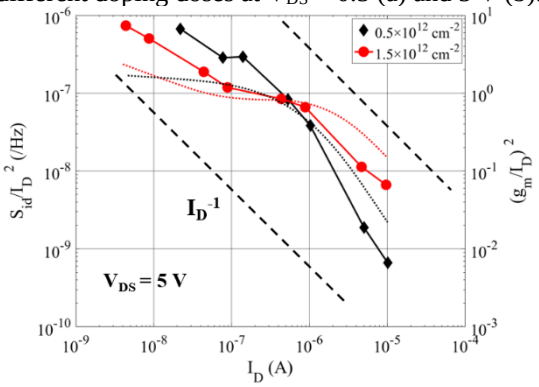

Fig.4 Normalized S_{id} / I_D^2 at 10 Hz (dots) and $(g_m/I_D)^2$ (dashed lines) as functions of I_D for counterpart TFET with Ohmic contacts for the 2 different doping doses at V_{DS} = 5 V.

DFT study of adsorption density of gas molecules in 2D materials

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Gas sensors are required in many fields, such as city air quality and emission, environmental monitoring or medical diagnostics [1]. 2D materials have become promising candidates to produce highly sensitive gas sensors due to their extraordinary properties [2], but they suffer from the disadvantage of having complicated manufacturing processes. Due to this inconvenience, it would be desirable to know, before fabrication, how well a specific 2D structure (monolayer, multilayer or a heterostructure) is going to perform in sensing a specific gas molecule. With this aim in mind, a modified version of the Langmuir adsorption model (derived from Statistical Mechanics, assuming non-localized adsorption) [3] coupled to Density Functional Theory (DFT) calculations has been developed to compute the density of adsorption of molecules in 2D structures. As an example of application NH_3 and N_2 adsorption in MoS_2 monolayer has been investigated, but the model is not limited to these systems.

First, in order to justify the hypothesis made in the model development, the height of the barriers that molecules experience when moving across the MoS_2 plane have been calculated. It can be seen in Figure 1 how the average thermal energy of NH_3 molecule at 300K is significantly larger than the height of the barriers, and the same behavior is observed for N_2 therefore, it is justified to assume that the molecules can move in the plane.

Numerous structural relaxations have been performed using DFT and the L-BFGS optimization algorithm as implemented in QuantumATK [4]. From these calculations, two preferred points for adsorption have been extracted for both molecules, referred to as ‘center’ and ‘Mo’ as shown in Figure 2. To study the orientations in which the molecules are adsorbed, ab-initio simulations have been performed to extract the interaction energy between the molecules and the monolayer of MoS_2 as a function of the angle between them (Figure 3a). In the case of NH_3 a single preferred configuration has been found, that with the hydrogen plane parallel to the monolayer (Figures 2a and 2c). This can be deduced by the fact that exist a single angle that significantly minimizes the interaction energy. For N_2 it has been extracted similar results, finding that most stable configuration is that in which N_2 line form an angle of 56° with the MoS_2 plane (Figure 2b and 2d).

Using the information obtained about the adsorption process, the density of adsorption of NH_3 and N_2 in a MoS_2 monolayer has been calculated applying the modified Langmuir model. From that model it can be deduced that [3]

$$\rho = \frac{N}{A} = \frac{p}{k_B T}\left(\frac{2\pi k_B T}{h^2}\right)^{-\frac{1}{2}}\left[\exp\left(\frac{-E_{ads}}{k_B T}\right)\sum_{n=0}^{\infty}\exp\left(\frac{-E_n}{k_B T}\right)\right],$$

where N is the number of adsorbed molecules, p is the partial pressure of the gas, E_{ads} is the depth of the potential well obtained in the interaction curves (Figure 3b), and E_n are the eigenvalues of the potential well (harmonic oscillator) in which the molecules are trapped. The obtained values for the two

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preferred adsorption sites, in the most probable orientation, are $\rho = 2.004 \times 10^{15}\ cm^{-2}$ in the case of NH_3 and $\rho = 2.513 \times 10^{13}\ cm^{-2}$ in the case of N_2 for T= 300 K and p = 1 atm. The variation of ρ with temperature has been calculated too, as can be seen in Figure 3c for NH_3 and Figure 3d for N_2.

The interaction between the monolayer MoS_2 and the NH_3 and N_2 molecules have been investigated with first principles calculations and the density of adsorption has been computed using a statistical mechanics-based model. We obtain that MoS_2 is ~80 times more sensible to NH_3 than N_2, a result consistent with the fact that N_2 is an inert gas.

This work paves the way for conducting new calculations employing different molecules and structures to determine the optimal sensing structure for detecting specific molecules.

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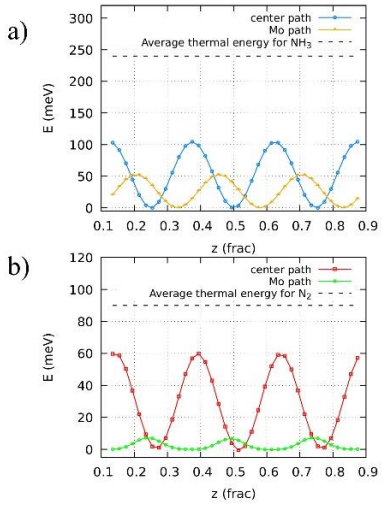

Figure 1. Potential barriers experienced by NH_3 a) and N_2 b) when moving across MoS_2.

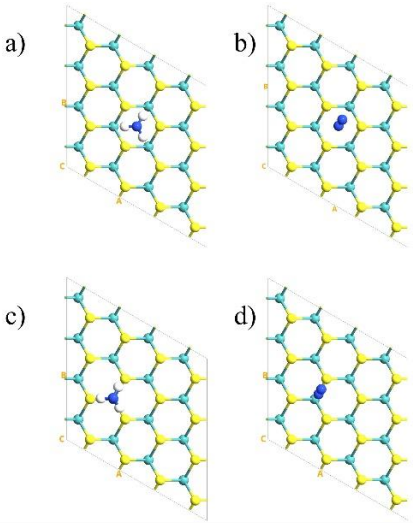

Figure 2. Center adsorption sites a) and b), and Mo adsorption sites c) and d).

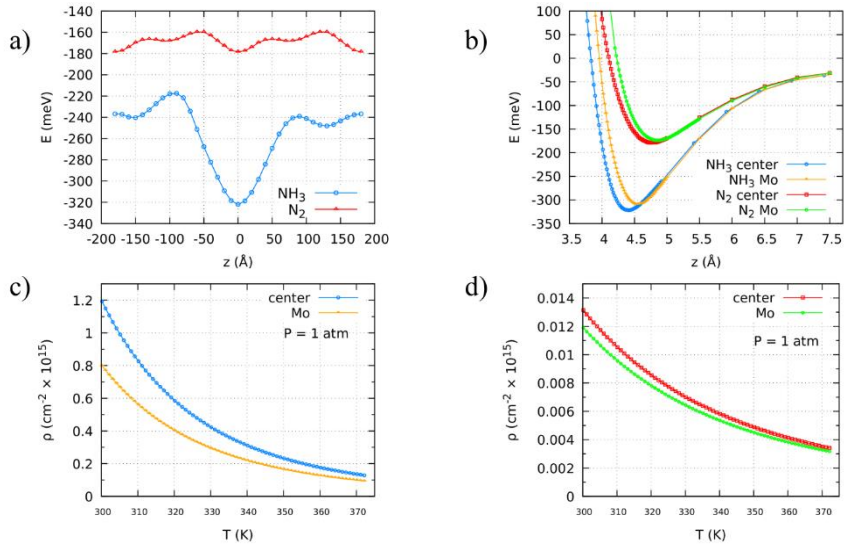

Figure3. Interaction energy as a function of the angle a) and vertical distance b) between the molecules and MoS_2, and variation of ρ with temperature for NH_3 c) and N_2 d).

Performance of Pulse-Programmed Memristive Crossbar Array with Bimodally Distributed Stochastic Synaptic Weights

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***Abstract*—In this paper, we present a method of implementing memristive crossbar array with bimodally distributed weights. The bimodal distribution is a result of pulse-based programming. The memristive devices are used for the weights and can only have an ON (logical "1") or an OFF (logical "0") state. The state of the memristive device after programming is determined by the bimodal distribution. The highly efficient noise-based variability approach is used to simulate this stochasticity. The memristive crossbar array is used to classify the MNIST data set and comprises more than 15,000 weights. The interpretation of these weights is investigated. In addition, the influence of the stochasticity of the weights and the accuracy of the weights on the classification results is considered.**

Keywords- artificial neural networks, memristive crossbar array, bimodal distribution, noise-based simulation, pulse-programming, variability

I. Introduction

Memristive devices (MDs) are non-volatile memories and are considered promising candidates for the development of hardware-based artificial neural networks (ANNs) [1][2]. The MDs can be in one of the two: states low-resistive-state (LRS) and high-resistive-state (HRS) [3]. During the SET process, the MD is switched to LRS, which corresponds to a logical "1". The RESET process switches the MD to HRS, which corresponds to a logical "0". The MDs exhibit stochastic fluctuations which result in device-to-device and cycle-to-cycle variability [4]. This stochasticity variability can be simulated using the Noise Based Variability Approach (NOVA) [5]. ANNs can be implemented as a memristive crossbar array, whereby a single cell, consisting of two MDs, functions as a weight with possible values from -1 to +1 [6].

II. Setup of the Memristive Crossbar Array and Programming Scheme

To classify the MNIST data set (images consisting of 28x28 pixels), the memristive crossbar array consists of 784 inputs, 10 outputs and 15,680 memristive cells (as in [5]). In the simulation, the MDs are considered as simple fluctuating resistors for simplicity. Two memristive cells are required to design a weight W between -1 and +1: one G^+ and one G^- cell (see Eq. 1 for calculation).

$$W = G^+ - G^- \qquad \text{Eq.1}$$

The required weight values come from the software training. The memristive cells are programmed by applying pulses, which can be changed in terms of amplitude, pulse width and number of pulses [7]. The starting point is that the weights are set via "probabilities". The MDs can only become the logical values "0" and "1" and their state changes with a certain "probability" depending on the pulses applied. Accordingly, their conductivity follows a bimodal distribution. For each applied pulse, the state of the memristive cell can be represented via a bimodal distribution (how many devices are statistically in the HRS and in the LRS) [8]. In [9] it is shown that the statistical variation resulting from a superposition of many bimodal distribution functions can be represented by the superposition of Gaussian distribution functions. This allows the replacement of the bimodal distributions with Gaussian distributions for the usage of NOVA to simulate the fluctuations of the MDs as in [5]. The simulations are carried out with the Spectre simulator Cadence Virtuoso. After the simulation, the winner is determined according to the winner-takes-all principle as in [10].

III. Interpretation of the Weight Definition from Pulse Programming

A pulse with a pulse width of 1 µs and an amplitude of 0.8V is defined for programming the devices. This pulse is sent 100 times to 128 different cells that are in the HRS before the first pulse. A MD can therefore be in the HRS state or in one of the 100 programming states depending on the number of applied pulses (measurement data from [7]). To be able to use NOVA, an average value and a standard deviation are calculated for each programming state using the 128 measured curves. According to Eq. 1, two MDs are required for a weight W, whereby a weight W can be composed according to figure 1 (a).

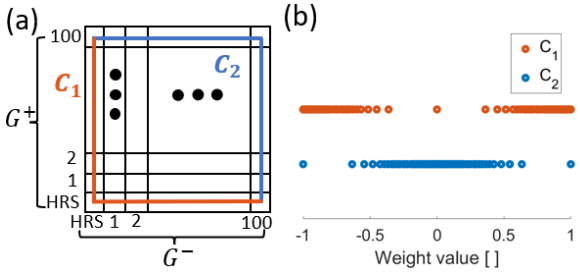

Figure 1 (a) Representation of the 10,201 possible weights within the -1 to +1 range in the 101x101 matrix via paths. (b) Possible discrete weight values within the -1 to +1 range depending on the selected path.

Paths (e.g. C_1 and C_2) can be formed within this matrix, which must be set for the range from -1 to +1 for G^+ and G^-. However, it is noticeable that the values of G^+/G^- do not increase continuously from HRS to the 100th pulse, which means that the values from -1 to +1 can also be set with different accuracy. This is illustrated in figure 1 (b). Here the path C_1 covers weight values in the range from -1 to -0.5 and +0.5 to +1 with high accuracy, whereby C_2 provides a higher resolution in the range from -0.5 to +0.5.

Figure 2 shows the standard deviation of each possible weight W. Here it can be seen that path C_1 has lowest standard deviations and C_2 has the highest standard deviations.

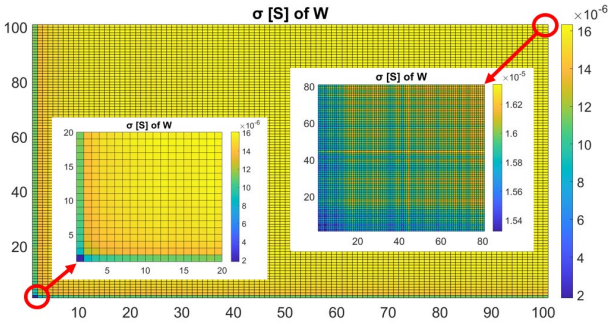

Figure **2** Visualization of the resulting standard deviation for each possible weight to be set.

IV. Simulation Results of the Memristive Crossbar Array

The memristive crossbar array is tested with the same images of a "7" and a "4" as from [5] (programming of weights by conductance level), as well as the image of a "1". For all cases, the weights are trained with a resolution of 0.1 weight stepping. The paths C_1 and C_2 are compared by adjusting the target weight to the closest possible value (see figure 1(b)). The results are shown in Table 1, as percentage of classifying the given number as a winner.

Table 1 Classification results of the images of a "7", "4" and "1" with path C_1 and C_2. The expected result is marked in green and the result with the highest probability is marked in blue.

Results	"7", C1	"4", C1	"1", C1	"7", C2	"4", C2	"1", C2
0	4.65%	23.94%	2.81%	7.73%	9.36%	4.45%
1	1.35%	6.94%	76.74%	6.28%	8.64%	15.48%
2	0.44%	0.36%	0.08%	11.17%	10.79%	9.13%
3	2.57%	1.10%	4.34%	12.11%	7.67%	11.00%
4	1.13%	8.52%	4.60%	8.14%	11.69%	8.57%
5	0.24%	0.88%	0.21%	9.73%	9.62%	9.39%
6	0.84%	16.15%	4.35%	6.00%	10.30%	10.60%
7	87.84%	32.58%	6.23%	20.68%	11.20%	12.00%
8	0.92%	9.39%	0.34%	9.74%	12.30%	10.26%
9	0.02%	0.14%	0.30%	8.42%	8.43%	9.12%

Table 1 shows that path C_2 delivers significantly worse classification results than path C_1. The reason for this is that the variability in the weights is very large for path C_2, which means that no precise classification is possible. The three digits are all classified with a similar probability. In contrast, in path C_1 the "7" is classified correctly with 87.84% (in [5] in the worst case 99.4% and best case 100%) and the "1" with 76.74%. The "4" is misclassified in most cases and is most frequently identified as a 7. In [5], this "4" is correctly classified in the best case with 50.44%.

Two factors play a role in the result of the programming: 1) The possible fluctuation of the desired weight value and 2) the number of adjustable weights or the accuracy of how finely resolved they should be set.

Path C_1 was selected for testing the "1" image, with weights set to increments of 0.1, 0.05 and 0.025 and noise levels of 100% (referred to the statistical variations as observed in the measurements), 85%, 67%, 25% and 0%. The results are shown in figure 3.

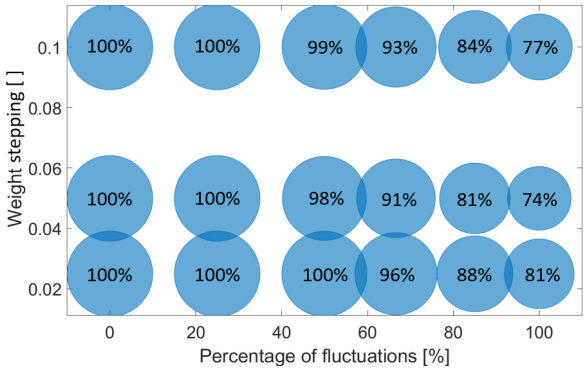

Figure **3** Illustration of the effect of different increments of the weights and a reduction in the variability of the weights. The percentage for the correct classification of "1" is given.

Figure 3 shows that the classification with a step of 0.025 is better than with 0.1, but the result only improves slightly. However, the 0.05 step is worse than with 0.1, as the finer discretization leads to weight combinations with an increased σ. It is noticeable that a reduction of the variability provides significantly better classification results. Even with a reduction of 1/3, the results are in the 90% range for all step sizes.

V. Conclusion

The programming via pulses shows strong variability in the weight values. As a result, the classification accuracy of the MNIST dataset is influenced by the variability depending on the G^+/G^- settings. In addition, regarding a high probability for a correct classification, it is more important that the weights fluctuate less than whether they can be set precisely. A reduction of the fluctuations observed in measurements by 33% already shows significant improvements. However, even without fluctuations a precise setting of conductance states is important to achieve the correct classification results.

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Interface Roughness in Resonant Tunnelling Diodes for Physically Unclonable Functions

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Counterfeiting costs the semiconductor industry billions annually[1], and Physically Unclonable Functions (PUFs)[2, 3] are a solution to this that has garnered interest, which works by uniquely identifying chips they are attached to. Resonant Tunnelling Diodes (RTDs) are one such device being investigated for PUF applications[2, 3]. PUFs depend on device variability to provide an unpredictable output response to a given challenge input, and multiple of these challenge-response pairs can compose a random and unique 'fingerprint', to identify devices against a database. Interface Roughness (IR) along heterostructure interface are one such source of stochastic variability of RTDs, which we have included by varying the GaAs/$Al_{0.3}Ga_{0.7}As$ interfaces in the 'smooth' 55nm×10nm×10nm RTD shown in Fig.1(a). This IR leads to $Al_{0.3}Ga_{0.7}As$ barriers as shown in Fig.1(b), and causes variation in both the quantum well[3] and barriers[4], which RTDs are highly sensitive to.

We carried out simulations using the custom and modular Nano-electronic Simulation Software (NESS)[5] software, using a Non-equilibrium's Green's Function (NEGF) solver to capture quantum tunnelling behaviour. 25 devices were randomly generated and simulated in the ballistic regime for different correlation length L_C and root-mean-square roughness asperity Δ_{RMS}.

Fig.2 displays colourmaps of PVCR and voltage and current standard deviations of resonant peaks, or local maxima. Δ_{RMS} has a greater effect on the parameters shown than L_C, and there seems to be a trade-off between decreasing Peak to Valley Current Ratio (PVCR) and increasing voltage and current standard deviations as Δ_{RMS} is increased. L_C =7.5nm and Δ_{RMS} =0.3nm balance PVCR with moderately large standard deviations, which fits the purpose of using RTDs as PUF components[2], by being able to encode information in whether the current and voltage of the resonant peak is greater or less than the centre of the current and voltage distributions. This also roughly matches the parameters used in [6], and Δ_{RMS}=0.3nm is close to the monolayer thickness of GaAs and $Al_{0.3}Ga_{0.7}As$.

Fig.3 shows the significant variability of current-voltage curves and distribution of resonant peak current-voltage peaks for L_C=7.5nm and Δ_{RMS}=0.3nm. We fitted with normal curves and used the mean of these to split the distribution into quadrants. With further simulations, it would be possible to assess the minimum bits of information that could be encoded in an RTD with min-entropy $-\log_2 n_{max}/N$. Here n_{max} would be the number of resonant peaks in the quadrant most densely populated as seen in Fig.3(b), and N the total number of devices. Multiple RTDs would then be combined on a chip to create a PUF encoding a certain amount of information[2] for identification.

We have explored how varying L_C and Δ_{RMS} for IR along GaAs/$Al_{0.3}Ga_{0.7}As$ interfaces in RTDs changes the mean PVCR and the standard deviations in resonant peak voltage and current values. It was determined that L_C =7.5nm and Δ_{RMS} =0.3nm balances PVCR with moderately large standard deviations, and briefly noted how this could be used to encode information quantified by min-entropy, allowing multiple RTDs be combined into a PUF. This research provides a direction for further research of RTDs for PUF applications.

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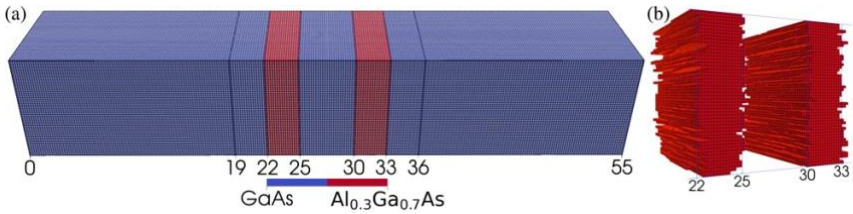

Figure 1: Fig(a) is a 'smooth' 55nm×10nm×10nm RTD composed of two 19nm long $2 \times 10^{18} cm^{-3}$ n doped GaAs source-drain regions and a central $5 \times 10^{15} cm^{-3}$ n doped region comprising two 3nm GaAs buffers, two 3nm $Al_{0.3}Ga_{0.7}As$ and a 5nm GaAs quantum well. Fig(b) shows $Al_{0.3}Ga_{0.7}As$ barriers with randomly generated IR of L_C=7.5nm and Δ_{RMS}=0.3nm, following an exponential roughness model[7].

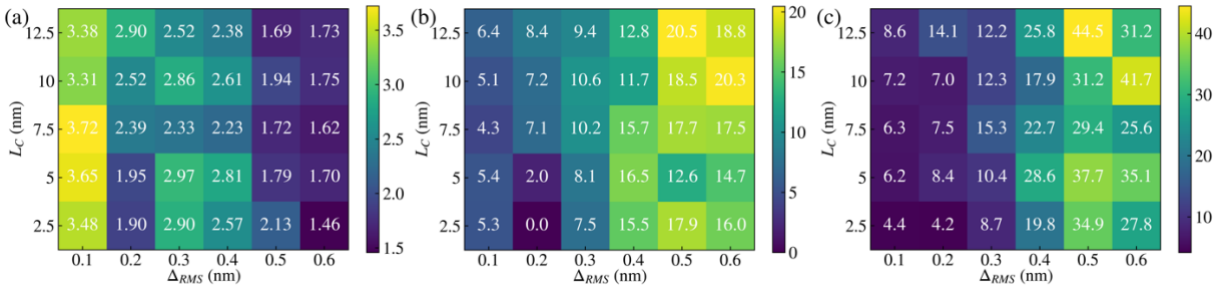

Figure 2: Colourmaps of distribution values for different L_C and Δ_{RMS}. Fig(a) is the mean of PVCR, and Fig(b) and Fig(c) are respectively the voltage (millivolts) and current (nanoampere) standard deviation of fitted normal curves to the distribution of the current-voltage of the local resonant peak values as seen in Fig.3.

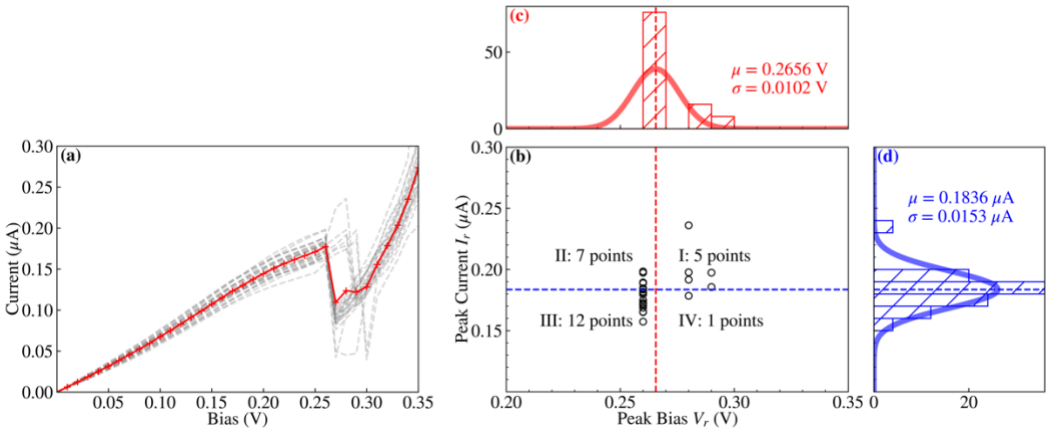

Figure 3: Fig(a) shows current-voltage plots for 25 randomly generated RTDs with exponential IR of L_C=7.5nm and Δ_{RMS}=0.3nm as grey dashed lines. The mean current-voltage characteristic is shown as a solid red line with plus markers. The resonant peak, or local maxima, of each current-voltage characteristic is shown in Fig(b) and is split into 4 quadrants by the mean of fitted normal distributions for the voltage and current distributions as seen in Fig(c) and Fig(d) respectively. Fig(c) and Fig(d) also show histograms for occurrence of resonant peak values.

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Influence of multiple MISHEMT conduction channels on analog behavior

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***Abstract* - In this paper, the multiple channels of a MISHEMT device (Metal/Si_3N_4/AlGaN/AlN/GaN - Metal-Insulator-Semiconductor High Electron Mobility Transistor) are studied regarding their impact on basic DC and RF figures of merit. Although most authors treat the 2DEG channel as the MISHEMT main channel, it is shown that its MOS channel contribution to the different RF parameters is of great importance. This unique characteristic makes the MISHEMT RF parameters to be dependent on both V_{GS} and V_{DS}. In relation to a pure 2DEG conduction, the MOS channel is responsible for a large set of analog parameters improvements. It offers an increase of up to 17.6 dB in S21 and of 23 dB in MAG, while sustaining a high f_T and f_{max} for a larger range of V_{GS} and drain current level.**

Keywords - MISHEMT; Multiple Channels; GaN; RF.

I. Introduction

Wide bandgap semiconductors have been widely used in power electronics [1, 2] due to their ability of operating at high frequencies [3] and at harsh environments [4, 5], showing high power gain at 10 GHz [6]. The GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) is one of the promising devices for power applications. In comparison to the HEMT, the MISHEMT also presents high current level, high breakdown voltage and reduced gate current leakage due to the gate insulator [2, 7].

The MISHEMT's heterostructure gives rise to a two-dimensional electron gas (2DEG) [8]. Although the 2DEG at the heterointerface is commonly treated as the main current channel of the MISHEMT, due to the device's gate insulator, depending on its gate biasing, it presents another current channel at the gate insulator/ semiconductor interface as well, whose contribution to the drain current directly influences the device behavior from DC point of view [9]. In this work, we propose the analysis of the basic analog parameters, i.e. intrinsic voltage gain (A_V), Early voltage (V_{EA}) and using the S-parameters, maximum available gain (MAG), unit gain frequency (f_T), maximum oscillation frequency (f_{max}) under the influence of the multiple MISHEMT conduction channels.

II. Device Characteristics

Experimental data was obtained by measuring a set of MISHEMTs fabricated in imec – Belgium. The device structures consist of a TiN/Si_3N_4 gate stack over a heterostructure of AlGaN/AlN/GaN grown on a silicon platform. The devices have a width of 40 µm with a W/L ratio of around 100, a 2nm thick insulator, a 15 nm thick barrier, 1 nm thick spacer layer and a 200 µm thick buffer. The RF devices have 2 gate fingers, like two MISHEMTs in parallel. The measured MISHEMTs differ on the distance between its gate and drain electrodes (L_{GD}), shown in Fig. 1, being one short (~750 nm), and one large (~2.5 µm). With a small L_{GD} both channels contribute greatly to drain current (I_D); with a large L_{GD} the MOS channel becomes limited to the gate electrode area, facing a higher series resistance, while the 2DEG extends even more, i.e. the channel length increases. In this case, the main contributor to I_D is the 2DEG. More fabrication details can be found in [1]. The MISHEMT DC electrical characterization was made using the Semiconductor Parameter Analyzer B1500 [10] and its RF characterization was performed using the Keysight PNA Network Analyzer N5227B [11] from 500 MHz to 70 GHz with 100 µm pitch G-S-G microprobes.

III. Results and Analysis

It is obtained that MISHEMT has a 2DEG channel with an activation voltage ($V_{GS} = V_{t\_2DEG}$) of -4.7 V. The 2DEG channel is distributed between two heterointerfaces, 1 nm distant from each other. At the Si_3N_4/ AlGaN interface it has an accumulation type MOS channel, with an activation voltage ($V_{GS} = V_{t\_MOS}$) of about -1.5 V [12]. Fig. 2 shows the MISHEMT electron concentration under a $V_{GS} > V_{t\_MOS}$ (a), when both 2DEG and MOS channels conduct, $V_{t\_2DEG} < V_{GS} < V_{t\_MOS}$ (b), where the MOS channel faces a high series resistance thus contributing less to I_{DS}, and $V_{GS} < V_{t\_2DEG}$ (c), when the device is shut off. These different conduction mechanisms (2DEG and MOS), shown in Fig. 2, make the MISHEMT capable of offering a higher intrinsic voltage gain (Av) for higher drain voltages (V_{DS}) as shown in Fig. 3, when 2DEG conduction is dominant in the saturation like region. Fig. 4 shows the I_D and transconductance (gm) as a function of gate voltage (V_{GS}). It can be seen that for the device with shorter L_{GD} there is a second increase in I_D for more positive V_{GS}. This is due to the increasing number of electrons in the AlGaN barrier layer and subsequent MOS channel activation, which can be observed in the multiple slope/peaks in gm.

Fig. 5 shows the scattering parameters for the input (S11) and for the output (S22) from 0.5 GHz up to 50 GHz for both devices under V_{DS} = 2 V and different V_{GS}. It is possible to see that for a smaller L_{GD}, S11 tends to be very predictable, while for a larger L_{GD} the input impedance is lower for more positive V_{GS}. The gate and drain capacitances influence more each other on the device with smaller L_{GD}, so its gate impedance has a behavior intertwined with V_{DS} and shows a smoother transition between different V_{GS}. For a large L_{GD} two specific impedance behaviors take place, one before V_{t_2DEG} and one after it, as it is dependent mainly on the 2DEG channel condition. For the larger L_{GD} device, when the 2DEG channel is in its full formation, the channel capacitive behavior attenuates, giving place to a primarily resistive characteristic. This is due to the 2DEG nature, which is made by free electrons detached from their original atoms. Since in this case the MOS channel plays a minor role in I_D, there is no more great change in the output impedance for V_{GS} > -3 V. The device with a short L_{GD} continues to show reasonable changes in S22, as the electrons in the bulk of AlGaN and at the MOS channel are very susceptible to external stress.

A comparison of the devices MAG at 2.4 GHz is shown in Fig. 6, and of transmission coefficient (S21) in Table 1. For more negative gate bias, the curves show that the 2DEG channel length does not affect MAG, which is reasonable because the 2DEG has a specific electron concentration. The MOS channel maintains a high MAG for V_{GS} > -3 V, since it is responsible for a new I_D increase for more positive gate bias. For the V_{GS} of interest of -1 V, where both channels are active in the device with shorter L_{GD} and only the 2DEG channel contributes to I_D of larger L_{GD} device, the increase in S21 for each volt increase in V_{DS} differs substantially for both devices, being bigger for the device with short L_{GD}.

A comparison of the devices f_{max} under different V_{DS} is shown in Fig. 7, and of f_T in Table 2. It can be observed that a shorter 2DEG channel length and the addition of MOS channel on conduction can substantially increase the device RF performance concerning its f_{max} for all gate bias range. The MOS channel can be pointed out as the responsible for extending the device RF performance in relation to f_{max}. Cutoff frequency also substantially increases when the MOS channel is included on conduction. These operation frequencies increase even more from large L_{GD} to short L_{GD} when V_{DS} is higher. The higher free electron movement is responsible for this behavior. When the MOS channel takes place over a great area of the 2DEG channel, it contributes to counter the internal polarizations, so the 2DEG electrons are not constantly being pushed towards the heterointerface.

Fig. 8 shows the f_T and f_{max} curves in relation to I_D for short and large L_{GD} devices. A mobility degradation phenomenon and a consequent gm reduction is observed for all curves with I_D > 20 mA. A short L_{GD} means that the overall channel length is also shorter, as the 2DEG channel is the sum of L_{GD} and MOS channel length. For I_D above 5 mA, the device with short L_{GD} shows a new increase in f_T, given that a shorter channel length presents a higher efficiency. Most of the f_{max} characteristics follow the same f_T behavior in this device, but f_{max} is higher for a larger I_D range. It is important to notice that, as the MOS channel activation offers a new rise in I_D and a new peak in gm, it contributes to a new increase in f_T for more positive V_{GS}.

IV. Conclusions

This work presents the analog behavior of MISHEMT with a large L_{GD} and short L_{GD} in order to analyze the impact of the multiple MISHEMT conduction channels. The device with short L_{GD} has significant MOS channel contribution while for large L_{GD} it can be considered negligible due to the high series resistance. The S11 shows that a pure 2DEG channel, when fully formed, starts to show a less capacitive behavior and more resistive behavior. The MOS channel, despite being commonly disregarded, plays a leading role on offering higher S21 (3.8 dB against -15.3 dB) and MAG (29 dB against 6 dB) for higher V_{DS}. It also offers high f_T and f_{max} values for a larger span of V_{GS} (from 2 V to 5 V for f_{max}) and I_{DS}. These features are possible due to the MOS channel contribution to new I_{DS} and gm rises.

Acknowledgment

The Brazilian authors acknowledge CNPq, CAPES and grant 2023/14492-4, São Paulo Research Foundation (FAPESP) for the financial support. We also thank Prof. Dr. Gustavo Rehder from LME/PSI/USP for the RF measurements.

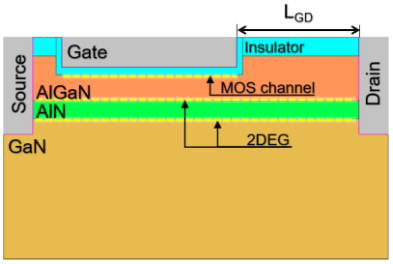

Fig.1 – MISHEMT schematic view.

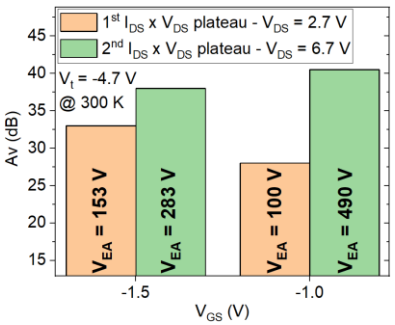

Fig. 3 – Intrinsic voltage gain and Early voltage for different bias conditions.

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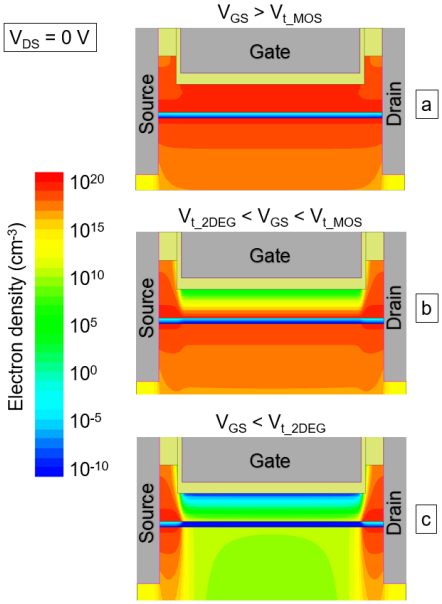

Fig.2 – Multiple channel conditions: 2DEG and MOS channels are enabled (a); 2DEG channel is enabled while MOS channel is disabled (b), and; 2DEG and MOS channels are disabled (c).

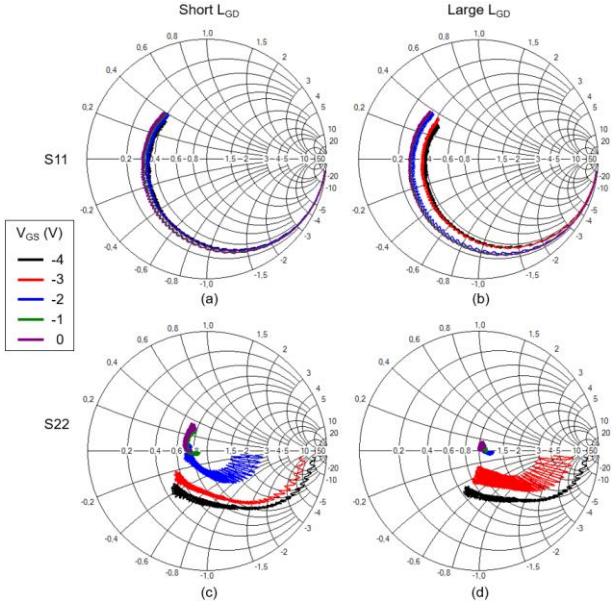

Fig. 5 – S11 for the MISHEMT with short L_{GD} (a) and with large L_{GD} (b). S22 for the MISHEMT with short L_{GD} (c) and with large L_{GD} (d).

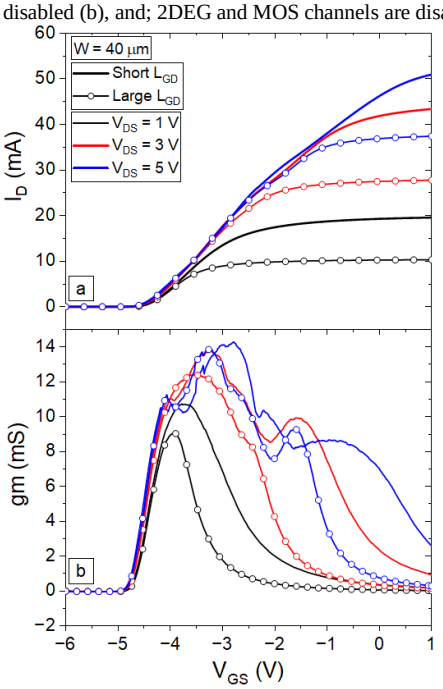

Fig. 4 – Drain current (a) and transconductance (b) as functions of gate voltage for short and large L_{GD} devices and different drain voltages.

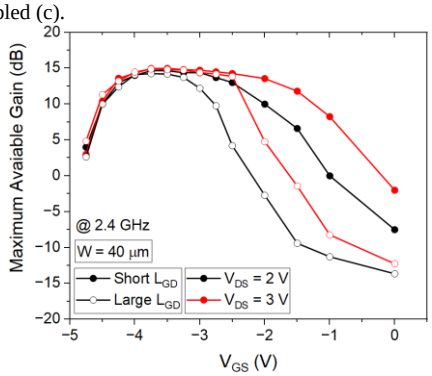

Fig. 6 – MAG as a function of gate voltage of short and large L_{GD} devices operating at 2.4 GHz for different drain voltages.

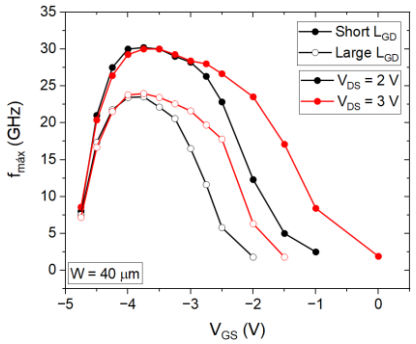

Fig. 7 – f_{max} as a function of V_{GS} of both short and large L_{GD} devices under different V_{DS}.

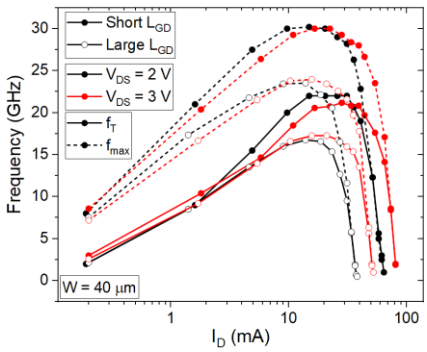

Fig. 8 – f_T and f_{max} as a function of drain voltage for short and large L_{GD} devices and different V_{DS}.

Table 1 – S21 values of short and large L_{GD} devices at V_{GS} = -1 V and different V_{DS}.

V_{GS} = -1 V	S21 for 2.4 GHz (dB)	
V_{DS} (V)	Short L_{GD}	Large L_{GD}
2	-12.0	-23.2
3	-2.0	-19.6
4	3.8	-15.3

Table 2 – f_T values of short and large L_{GD} devices at V_{GS} = -1 V and different V_{DS}.

V_{GS} = -1 V	f_T (GHz)	
V_{DS} (V)	Short L_{GD}	Large L_{GD}
2.0	3.0	0.5
3.0	8.6	1.0
4.0	12.6	2.0

Optimizing Unconventional Trilayer SOTs for Field-Free Switching

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Spin-orbit torques (SOT) provide rapid and energy-efficient manipulation of magnetic states in emerging spintronic devices [1]. Conventional SOTs, generated through the spin Hall effect (SHE) in the bulk and the Rashba-Edelstein effect (REE) at the interface in non-magnet (NM)/ferromagnet (FM) bilayers, have proven successful in switching logical states in SOT magnetoresistive random-access memory (SOT-MRAM). By utilizing perpendicular magnetic anisotropy, these devices can achieve sufficiently high densities to challenge conventional memories such as SRAM. However, due to the symmetry of conventional SOTs, reversing a perpendicular magnetic state is challenging without additional assistance, such as an external magnetic field. A promising approach involves leveraging unconventional SOTs in FM/NM/FM trilayers to break this symmetry [2]. By introducing a second FM layer below the NM, additional spin currents can be obtained through spin-orbit coupling (SOC) in the FM bulk and the FM/NM interface, offering enhanced control over the resulting SOTs compared to bilayers.

We investigate unconventional SOTs in trilayers to identify optimal configurations for achieving field-free switching of perpendicularly magnetized FMs. We consider a FePt/Cu/CoFeB trilayer with an in-plane electrical current and CoFeB magnetization along the high-symmetry direction, along which the bilayer torques vanish. In the FePt bulk, spin currents are generated through the anomalous Hall effect (AHE) and anisotropic magnetoresistance (AMR) [3]. We compute spin currents generated through the REE, by considering spin-dependent scattering from a Rashba SOC potential at the FePt/Cu interface. We include the three spin current contributions in a spin drift-diffusion model, and calculate the SOTs acting on the CoFeB layer. Figure 1 illustrates the dependence of the SOTs on the FePt magnetization direction, revealing a strong angular dependence of the torques. In particular the REE is most pronounced, when the magnetization aligns with the current direction, suggesting it could be the dominating mechanism for magnetization reversal in CoFeB/Ti/CoFeB trilayers [4]. Figure 2 depicts the thickness dependence of out-of-plane spin torques on the FePt and Cu thickness. We observe that AHE and AMR torques increase with FePt thickness, reaching saturation points based on the spin-diffusion length, similar to the SHE.

In conclusion, we demonstrate that FePt/Cu/CoFeB trilayers can generate unconventional SOTs acting on the CoFeB layer, tunable by the FePt magnetization direction. Our spin drift-diffusion approach enables the study and optimization of SOTs concerning materials, layer thickness, and magnetization directions. Ultimately, coupling the computed torques with the Landau-Lifshitz-Gilbert equation is essential for investigating the resulting magnetization dynamics in order to demonstrate deterministic field-free switching.

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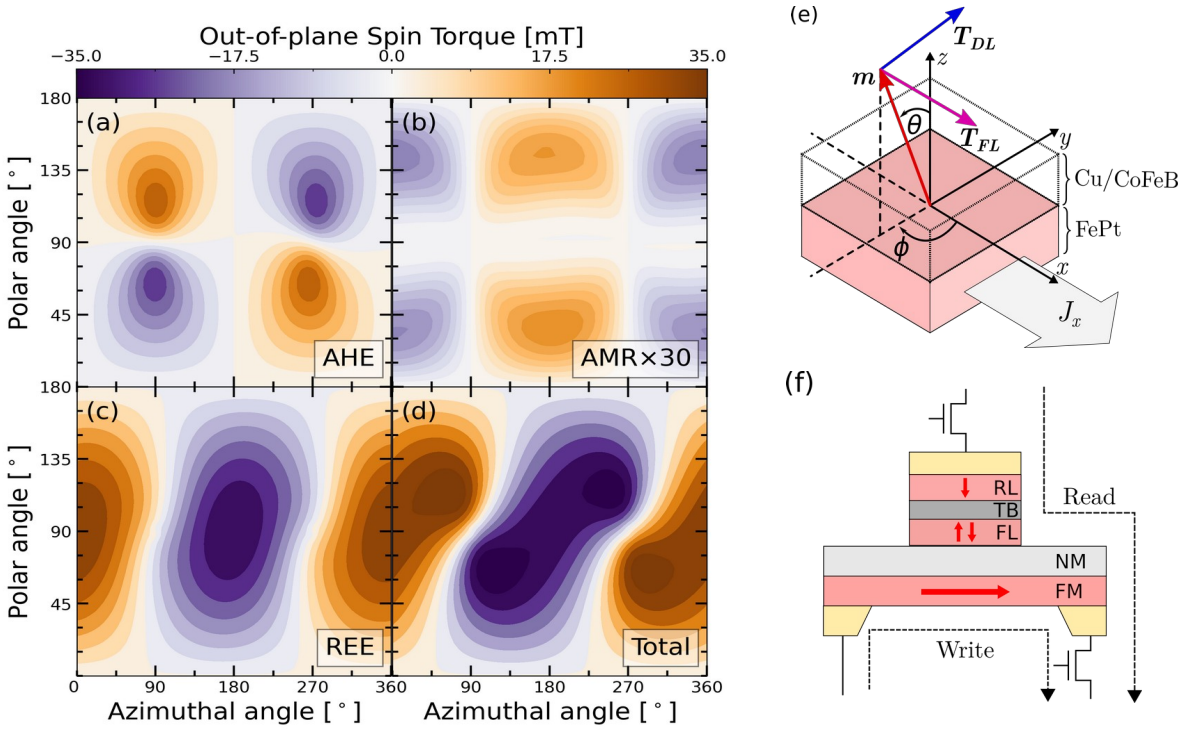

Figure 1: Out-of-plane spin torque in a FePt(10nm)/Cu(1nm)/CoFeB(1.2nm) trilayer, depicted in (e), as a function of the magnetization orientation of the FePt layer. A $5x10^{12}$ A/m² electrical current runs along *x*. The CoFeB magnetization is fixed along the -*y* direction, where conventional bilayer spin torques vanish. Panel (a), (b), (c), and (d) show the contributions from the AHE, AMR, REE, and total torque, respectively. A sketch of a SOT-MRAM cell based on the trilayer torques is shown in (f).

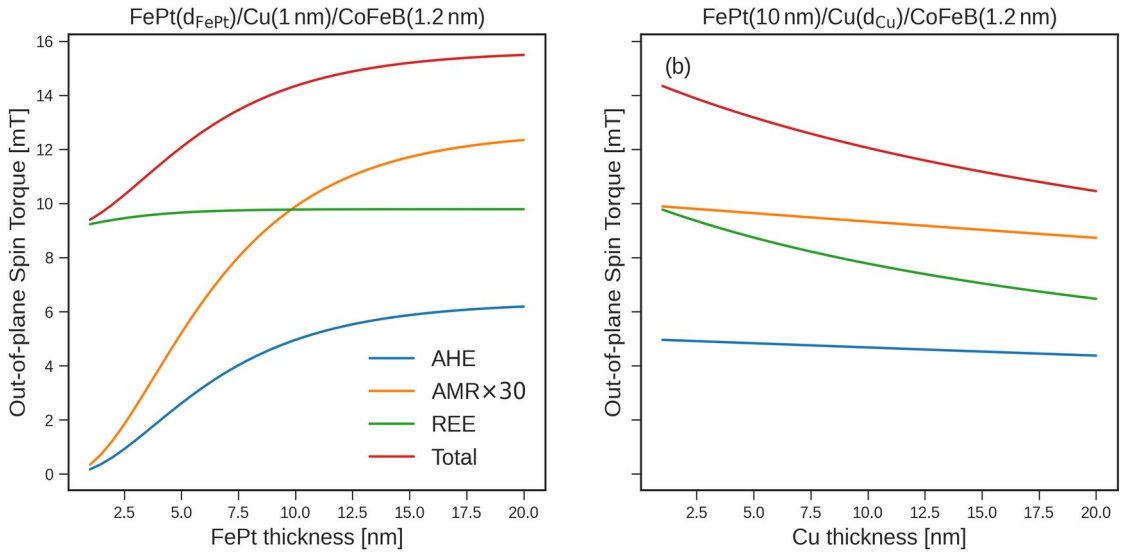

Figure 2: Dependence of the out-of-plane spin torque on the thickness of the FePt (a) and Cu layer (b) for the system depicted in Fig. 1(e). The FePt magnetization direction is given by θ = 60° and ϕ = 95°. The CoFeB magnetization direction is along -y.

Electron mobility in silicon under high uniaxial strain

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In the pursuit of enhancing the performance of semiconductor devices, the manipulation of material properties through strain engineering has emerged as a promising avenue [1]. In this work, the enhancement of the electron mobility in silicon has been experimentally investigated for uniaxial strain up to 1% applied along the [100] crystal direction.

A four-point bending setup is used to apply strain levels ranging from 0 to 1%, by steps of 0.02%, on an n-type silicon strain gauge supplied by *Kyowa* bonded on polycarbonate substrate (see inset Fig. 2a). A metallic strain gauge from *Micro-Measurements* is put next to the semiconductor one to measure the strain applied by the bending equipment. The device resistance has been obtained from current-voltage measurements using an *Agilent 4145* semiconductor analyzer in a voltage range from -0.5 V to 0.5 V with 20mV steps. To complement the experimental measurements, first-principles calculations have been conducted to determine the splitting of the conduction bands and the changes in the effective masses of the electron valleys induced by the strain. The theoretical calculations are based on density-functional theory (DFT) to obtain the band energies and effective masses, as implemented in ABINIT [2] with the generalized-gradient approximation (GGA) from Perdew-Burke-Ernzerhof (PBE) [3]. The uniaxial stress applied along the [100] crystal direction lifts the degeneracies of the six electrons valleys. The energy of the two Δ_2-valleys oriented along the strain direction increases, while the energy of the four others, called Δ_4-valleys, transverse to the applied stress, decreases with the strain as shown in Fig. 1a. On the other hand, the longitudinal effective mass increases (resp. decreases) for the Δ_2-valleys (resp. Δ_4-valleys) while the transverse one decreases (resp. increases) as shown in Fig. 1b.

The experimental results shown in Fig. 2a have been obtained from 2mm-long silicon beams with a cross-section of 250 µm by 20 µm, oriented transversely and longitudinally to the strain direction. The devices are n-doped and their doping level is about 10^{17} cm^{-3}. The mobility variations extracted from the raw measurements are shown in Fig. 2b and compared to the analytical model developed by Dhar *et al.* [4] and used by Ungersboeck *et al.* [5]. This work extends the original model by considering the variations of the effective masses, in addition to the valley splitting. The updated model enhances agreement with experimental data obtained from silicon beams and is then used to determine the undoped behavior. This is especially noticeable in the transverse contribution, where the reduction in mobility is offset by an increase in the transverse effective mass of the electron valleys. A significant improvement in the longitudinal component is observed at high strain, which was underestimated in the previous study.

To the best of our knowledge, this is the first time that the electron mobility variations at high strain have been observed experimentally in silicon for uniaxial stress applied along the [100] direction. The measurements have also validated the theoretical analysis, which extends beyond the existing model based solely on the splitting of valley energies due to strain.

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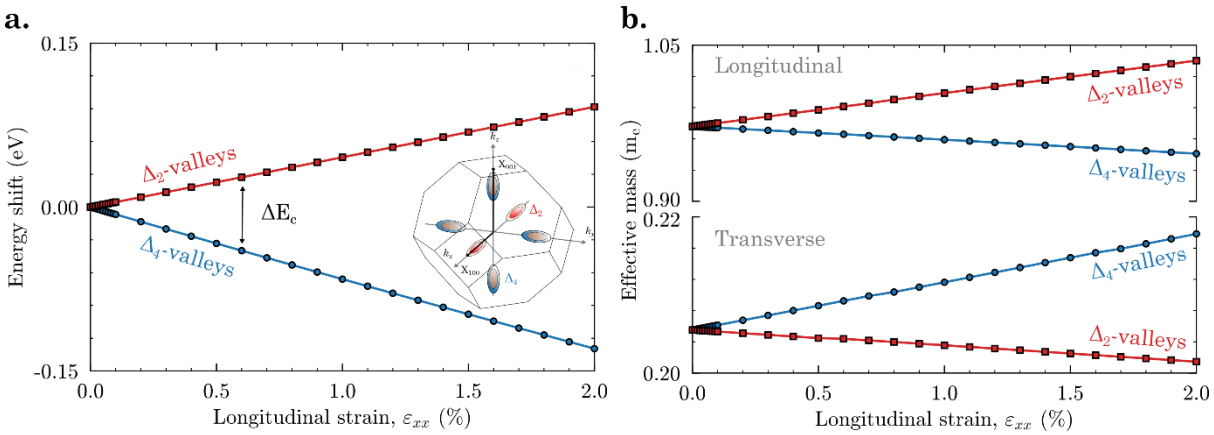

Fig. 1. (a) The energy shift of the minima of the electron valleys due to uniaxial strain along the [100] direction. The energy of the two valleys parallel to the strain (Δ_2-valleys in red squares) increases with the strain, while the one of the four valleys perpendicular to it decreases (Δ_4-valleys in blue dots). The inset shows the reciprocal space with the equipotential surface of the six electron valleys. (b) The effective masses for the Δ_2-valleys (red squares) and the Δ_4-valleys (blue dots) are given in terms of the free electron mass me. Both longitudinal (top) and transverse (bottom) masses are included.

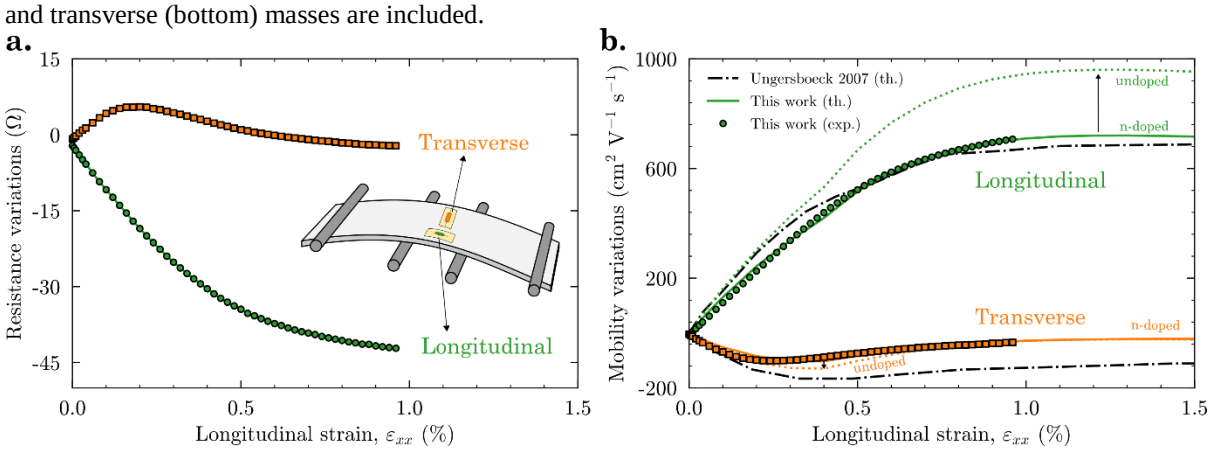

Fig. 2. (a) The resistance variations of the n-doped silicon beam were measured in both parallel (green dots) and perpendicular (orange squares) orientations to the strain direction. The picture depicts the four-point bending scheme used to strain the devices. Mobility variations were computed from the resistance measurements for the longitudinal (green dots) and transverse (orange squares) components. The figure displays the analytical model from Ungersboeck et al. [5] for undoped silicon as a dash-dotted line. The continuous and dotted lines represent the extended model for doped and undoped silicon, respectively, taking into account the effective mass variations.

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Towards ALD-grown MoS_2 devices for CMOS BEOL

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The achievement of isolated graphene in 2004 [1] by Geim and Novoselov has significantly boosted research in two-dimensional (2D) materials. Among the most promising 2D materials for the next electronic nodes are the transition metal dichalcogenides (TMDs), which present [2]: i) suitable bandgaps to be compatible with CMOS technology, ii) large effective masses reducing source-to-drain tunneling, iii) controllable thicknesses at the atomic level allowing excellent electrostatic control. However, difficulties in their fabrication such as the scarcity of scalable fabrication methods [3] still suppose a bottleneck for their industrial implantation. Despite the synthesis of these materials appearing simple, the use of high-temperature synthesis methods such as chemical vapor deposition (CVD) are forbidden in the direct 2D material growth on top of already processed silicon CMOS circuits. This fact obligates to use a mandatory layer-transfer process after growing the 2D material on a sacrificial substrate. On the other hand, atomic layer deposition (ALD) enables precise control over the thickness of the deposited layers due to a two-phase self-limiting process, conducted at relatively low temperature (100-400ºC). This temperature range is compatible with the back-end-of-line (BEOL) of CMOS technology [4]. Nevertheless, this low temperature may also cause poor crystallization and small grain size in the 2D layer, potentially limiting the carrier mobility and device performance [5].

We present MoS_2 back-gated devices synthesized via ALD through $[(NtBu)_2(NMe_2)_2Mo]$ and H_2S precursors [6]. The process was carried out directly on Si/90nm-SiO_2 wafers (100 mm) controlling the final MoS_2 thickness as a function of the number of cycles at a fixed temperature of 370ºC. The various wafer colors depicted in Figure 1.a are indicative of diverse deposited layer thicknesses and absorbance properties. The confirmation of the synthesized MoS_2 layer was performed through Raman characterization as illustrated in Figure 1.b. The spectrum exhibits three characteristic peaks: one appearing around 509 cm^{-1}, associated with the presence of Si/SiO_2 beneath the MoS_2; and the two peaks corresponding to the in-plane (E_{2g}) and the out-of-plane (A_{1g}) vibrational modes produced by 2H-MoS_2 crystals. Regardless the number of cycles employed in the synthesis, the peaks exhibit a separation of 24 cm^{-1}, indicative of a multi-layer material. In Figure 1.c, the atomic force microscopy topography of an etched device corroborates the presence of an approximately 10 nm-thick MoS_2 layer in a 90-cycles sample. Evaluation of the MoS_2 sheet resistivity was directly carried out through 4-probe characterization without any processing. Sheet resistance divided by the form factor ($F \sim \pi / \ln(2)$) [7] as a function of the synthesis parameters is shown in Figure 1.d suggesting resistivities in the MΩ range. Note that the sample is characterized at zero back-gate bias. Increasing the number of cycles and reducing the synthesis temperatures seems to conduct a material conductivity improvement.

To create back-gated devices, we employed standard photolithography with a metal (Cr/Au) lift-off process and SF_6 selective etching. Unfortunately, due to layer delamination (a common issue with these 2D materials [8]), only few structures were available. Initial electrical characterization of the back-gated devices revealed interestingly symmetrical output characteristic (Figure 2.a) and a prominent p-type branch (Figure 2.b). Significative gate leakage and the absence of photocurrent phenomenon were reported. Additionally, considerable hysteresis in the double gate swept, related to the interface traps,

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were observed. These advances open the door to optimizing the layer thickness and lithography process for scalable and CMOS-compatible ALD-grown MoS_2 transistors.

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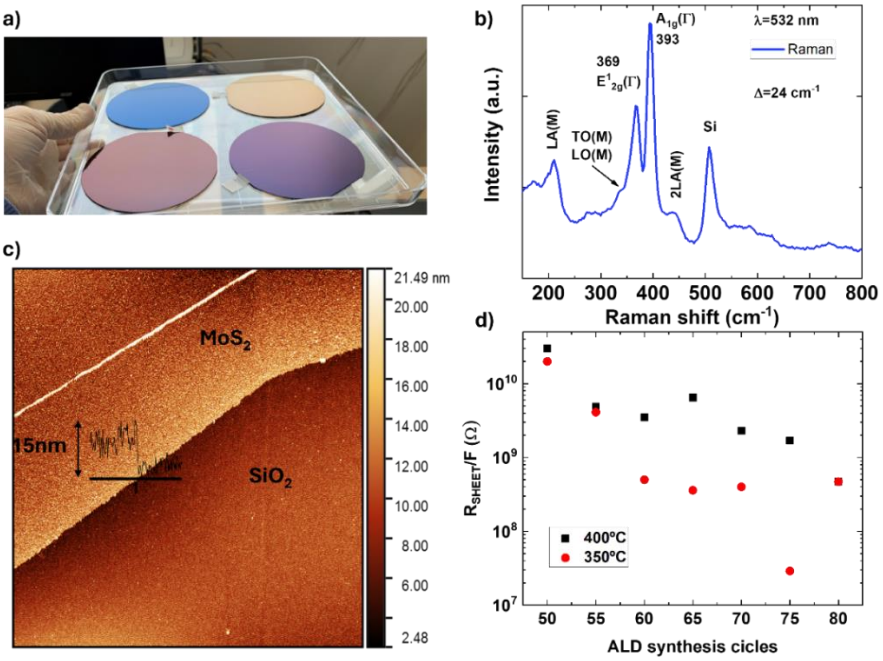

Figure 1: a) ALD-grown MoS_2 layers with increasing number of cycles (from left-bottom corner to left-top corner) on 100mm SiO_2/Si wafers. b) Raman spectrum for a 90 cycles MoS_2 layer. c) AFM topography of an etched area. d) Four-probe sheet resistance for different number of cycles and temperature.

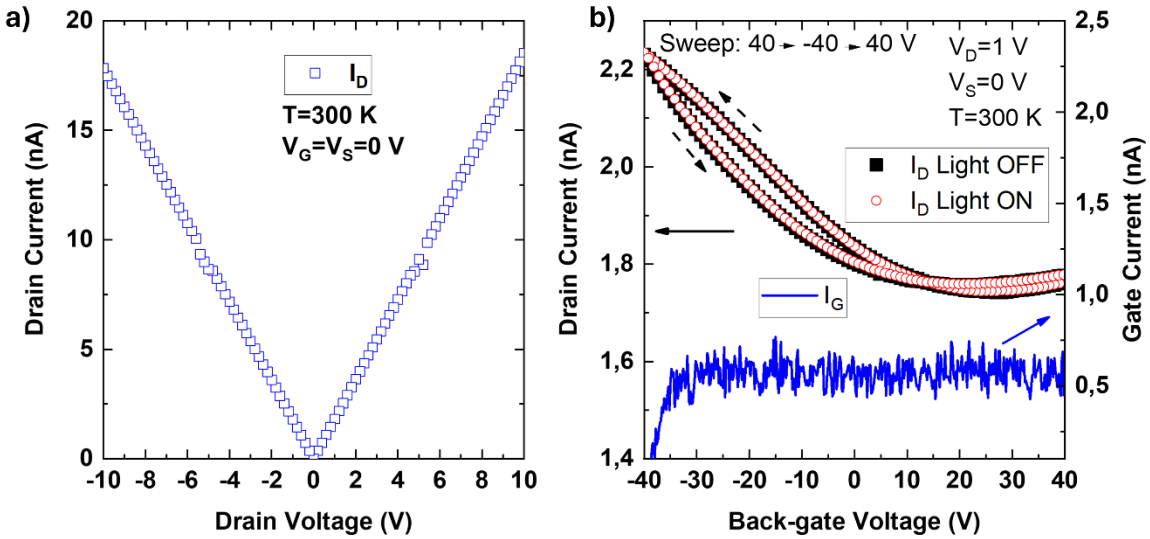

Figure 2: Output a) and transfer b) characteristics for a back-gated MoS_2 device synthesized at 370ºC with 90 ALD cycles. Light corresponds to artificial microscope light conditions. L=45 µm, W=100 µm.

Back Bias Effect with Hysteresis in Cryogenic 200 nm SOI MOSFETs

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Introduction Quantum computers, such as superconducting and spin-based, control qubits at millikelvin temperatures from room-temperature control systems, but problems such as the physical limits of wiring and heat influx arise when making more multi-qubits. Therefore, placing CMOS integrated circuits (cryo-CMOS) in cryogenic environments has recently attracted attention. The cryo-CMOS must also operate with low power consumption due to meet the refrigerator's cooling budget. SOI MOSFET technology is the promising candidate to reduce the power consumption because it has a back gate that can reduce the threshold voltage (V_t), even with V_t increasing at low temperatures. Previous work also shows the possibility of the low power with SOI MOSFET [1]. This study focuses on the back gate effect of SOI MOSFET and reports new finding of hysteresis effects.

Device Structure and Measurement Results Fig. 1 shows the device structure and parameters of the N-channel SOI MOSFET. The devices were fabricated using LAPIS Semiconductor 200 nm SOI CMOS process. We prepared two types of devices, RV_t (Regular V_t) and LV_t (Low V_t), in which the V_t's were controlled by varying the impurity concentration.

Fig. 2 shows the temperature and V_{sub} dependence of the LV_t device. V_t increases with decreasing temperature, and the increased V_t is then compensated by V_{sub}. Fig. 3 and 4 show the results of continuous measurements (two cycles) of V_{sub} = 0–10 V at 3 K. In the second measurement (2nd), the characteristics of the subthreshold region at V_{sub} = 0–4 V differ from those of the first measurement (1st). Fig. 5 shows the maximum V_{sub} and ambient temperature dependence. The hysteresis gradually disappears when the maximum V_{sub} is decreased and the temperature is increased. Fig. 6 shows the verification of the conditions under which the device returns to its 1st state. The hysteresis does not occur when there is a long interval between the 1st and 2nd measurement or the temperature was raised to 300 K, and then the 2nd measurement was carried out.

Discussion We consider that the above results are caused by the traps of the Box side, which only works at cryogenic temperatures. When the Box side is strongly inverted (V_{sub} < 8 V) at cryogenic temperature (< 10 K), carriers flowing to the back gate side could generate traps, and also carriers are trapped (Fig. 7(a)) and these induce the hysteresis effect (Figs. 3–5). However, the trapped carriers are detrapped depending on the return action to room temperature and the interval time (Fig. 6). The shoulder shape characteristics suggest the presence of low V_t locations within the device, which could be caused by the hole trap as shown in Fig. 7(b).

Conclusion We found out that the back bias in the cryogenic SOI MOSFET induced the hysteresis effect. This phenomenon must be considered in circuit design and parametric tests.

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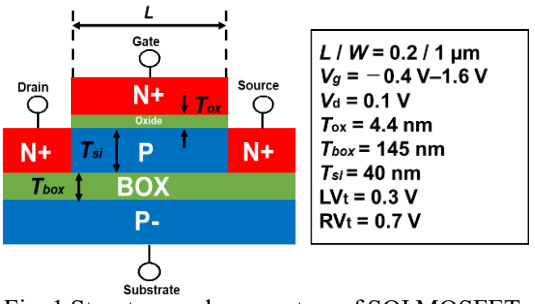

Fig. 1 Structure and parameters of SOI MOSFET.

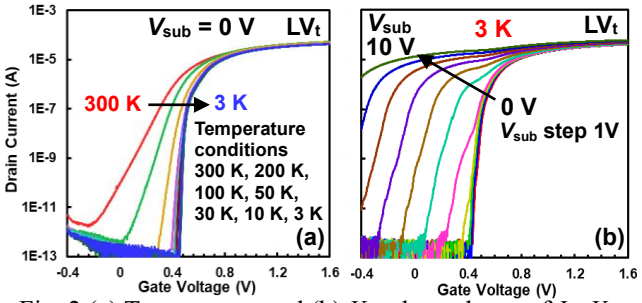

Fig. 2 (a) Temperature and (b) V_{sub} dependence of I_d–V_g.

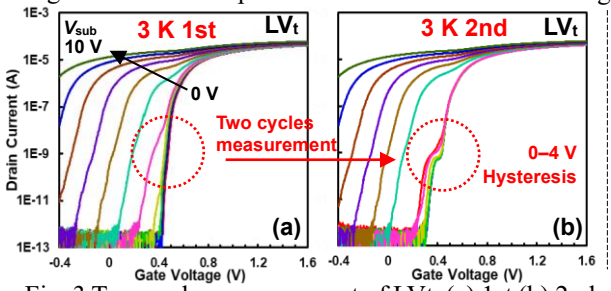

Fig. 3 Two cycles measurement of LVt. (a) 1st (b) 2nd.

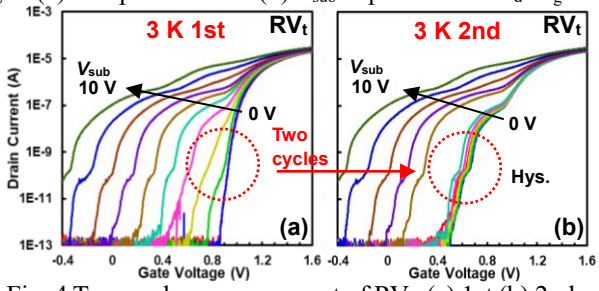

Fig. 4 Two cycles measurement of RV_t. (a) 1st (b) 2nd.

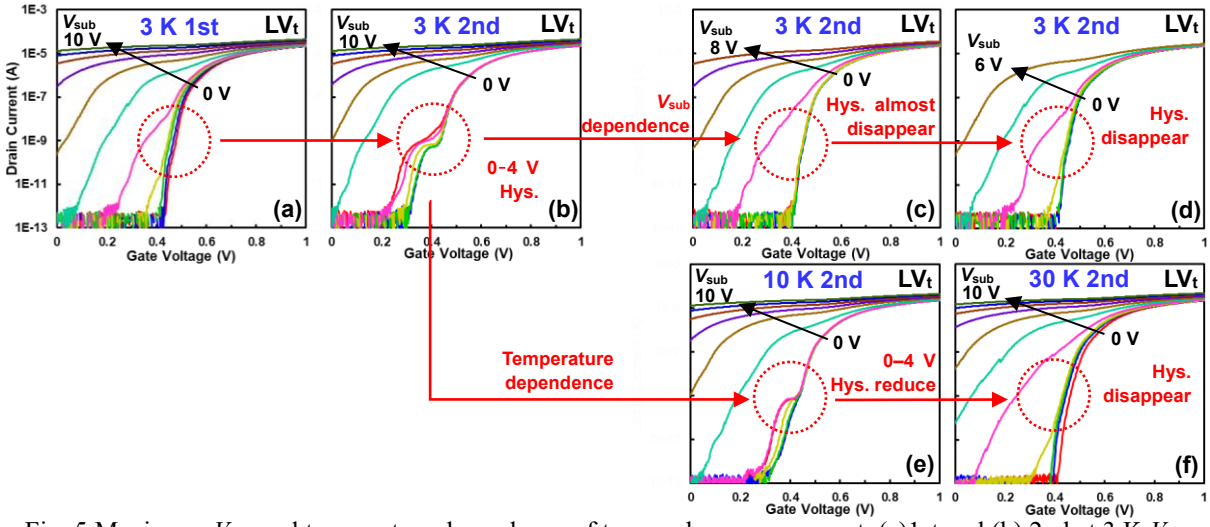

Fig. 5 Maximum V_{sub} and temperature dependence of two cycles measurement. (a)1st and (b) 2nd at 3 K V_{sub} = 0–10 V. (c) V_{sub} = 0–8 V 2nd and (d) V_{sub} = 0–6 V 2nd. (e) 10 K 2nd and (f) 30 K 2nd.

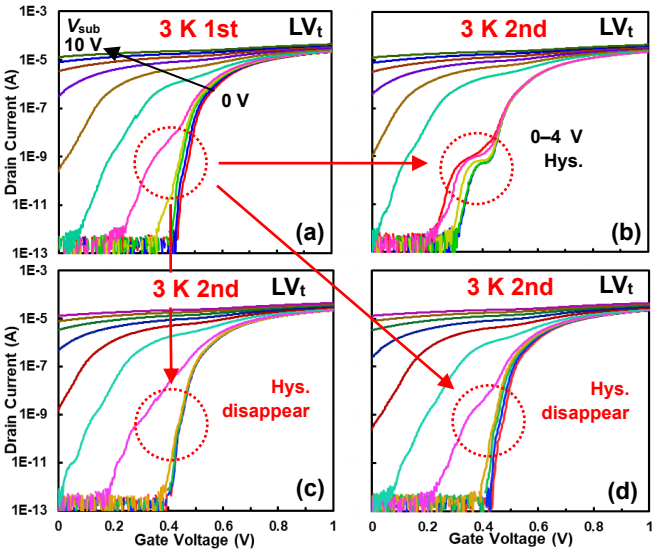

Fig. 6 Two cycles measurement (a) 1st, (b) 2nd, (c)with interval time (approximately 6 hours), and (d) via room temperature (300 K).

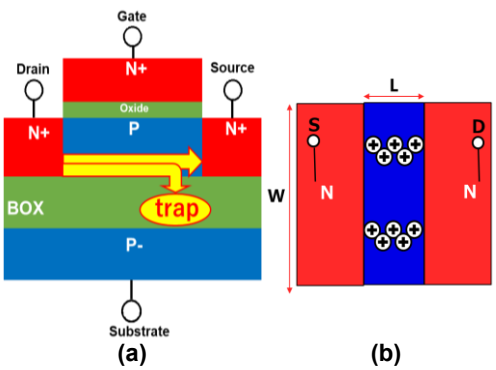

Fig. 7 Illustration of expected mechanism. Trap is generated when substrate bias is applied (a). Trap location dependence (b).

Reservoir computing for real-time arrhythmia detection using volatile and non-volatile low power memristors

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The development of disruptive artificial neural networks (ANNs) endowed with brain-inspired neuromorphic capabilities is emerging as a promising solution to deal with the challenges of the Big Data era, which requires large and complex software-based processing systems. Thus, the fabrication of robust and low power ANNs is of particular importance for the implementation of edge computing applications. More specifically, Reservoir Computing (RC) systems, which are based on Recurrent Neural Networks (RNNs) are able to handle temporal input data and transform them into a higher spatiotemporal dimensional feature space [1]. These properties combined with the fact that only the output layer requires training, as the reservoir block utilizes the short-term memory properties of the volatile devices that make it up, make RC systems ideal for applications where the input data are time-dependent and for applications where real-time decisions are critical [2].

This study focuses on the development of memristive devices that exhibit volatile and non-volatile switching operations. These operations are important for their utilization in the reservoir block, where the short-term memory effect and the relaxation time are used and for the final readout layer, where the conductance update is applied to the memristors of the crossbar architecture structure (CBA) [3]. It is thus apparent that the development of memristive elements with tunable properties is desired for the implementation of reconfigurable neuromorphic applications. For this reason, the impact of the bottom electrode (BE) material on the (non-)volatile behavior of the device was by using different materials such as BE (Pt NPs, ITO, n^{++} Silicon, TiN, and W). From our analysis, it was demonstrated that the thermal conductivity of the material directly affects the volatile mode of the devices. Concretely, the utilization of electrode materials with relatively low thermal conductivity values (< 20 $Wm^{-1}K^{-1}$) yielded the manifestation of a purely volatile mode (i.e. no retention). On the contrary, when electrode materials with relatively high thermal conductivity values were used (>30 $Wm^{-1}K^{-1}$), only a stable non-volatile mode was recorded. Interestingly, the co-existence of both modes was captured using electrode materials with intermediate thermal conductivity values. Figure 1 depicts the samples' performance and the respective switching modes. It is evident that sample A (Ag//SiO_2/Pt NPs) operate under the volatile mode as they switch from the LRS to the HRS before the polarity of the applied voltage is changed, in contrast to sample B (Ag/SiO_2/TiN) which remains at the low resistance state and switches to the high resistance state when the applied voltage is -0.4 V. The behaviors of samples A and B were used to develop two simulation models.

We utilized these models to develop an RC system, where the reservoir block consists of volatile memristors (simulation model of sample A) and the crossbar of non-volatile ones (simulation model of sample B). This system was used for heartbeat monitoring and arrhythmia detection, illustrated in Figure 2. For the implementation, we used different samples of heartbeats acquired from MIT-BIH

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heart arrhythmia database, in which we performed a normalization pre-processing and converted them into binary. These pulses have been sampled at 72 time points and by applying a 6-bit pulse stream resulted in the creation of 12 different sets of pulses with voltage amplitude of 0 and 1 (six pulses in total length). These pulse trains are applied to each volatile memristor, whose response is fed to each word line of the CBA. The RC system was able to successfully classify the heartbeat pulses as regular and arrhythmic and has an 81.58% recognition accuracy over the test set, while using only 48 non-volatile synapses and 12 reservoir threshold memristors, highlighting the high-level capabilities and extremely low power need of RC-based systems. By minimizing the bit pulse stream (2-bit) we can achieve recognition with accuracy reaching 85%, thus increasing the number of reservoir memristors, memristive synapses and power consumption.

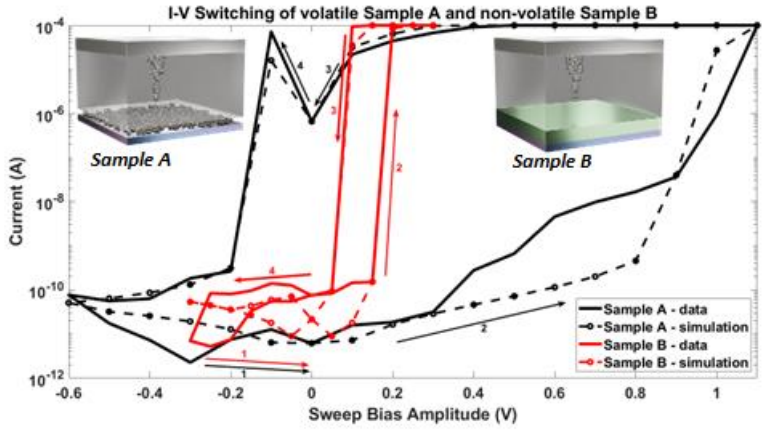

Figure 1 DC Sweep performance of volatile Sample A and non-volatile Sample B. The dot lines correspond to the simulation models.

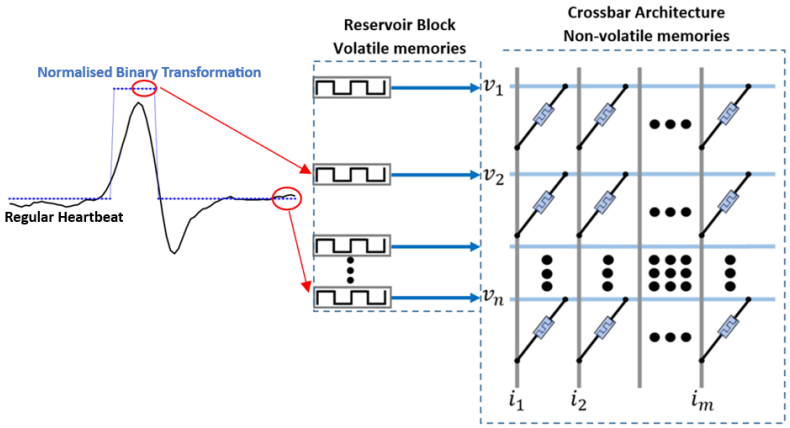

Figure 2 Demonstration of the RC system for heart arrhythmia detection.

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Interlayer Exchange Coupling for Enhanced Performance in Spin-Transfer Torque MRAM Devices

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Spin-transfer torque magnetoresistive random access memory (STT-MRAM) is revolutionizing nonvolatile storage with its broad application and data density benefits, driven by the magnetic tunnel junction (MTJ) with a CoFeB-based structure. Despite its advantages, miniaturization introduces reliability issues like back-hopping [1]. Our research focuses on the interlayer exchange coupling (IEC) in MTJs, crucial for magnetic alignment and device performance, aiming to optimize MTJ configurations for advanced memory technologies [2].

Magnetization dynamics in spintronics is defined by the Landau-Lifshitz-Gilbert (LLG) equation. IEC, critical for these dynamics, introduces a free energy density related to the angle $\Delta\emptyset$ between adjacent layer magnetizations as $E = J_1 cos(\Delta\emptyset) - J_2 cos^2(\Delta\emptyset)$ [3]. The constants J_1 and J_2 indicate the coupling strength and type (ferromagnetic or anti-ferromagnetic). Considering only the bilinear coupling term, the above expression simplifies to $E = J_1 cos(\Delta\emptyset)$. This formulation is essential for simulating IEC effects using finite element method (FEM) simulations, guiding the boundary conditions for accurate modeling of magnetic interactions within MTJs.

Exploratory simulations on the impact of IEC on various MRAM cells, depicted in Fig. 1, indicate that the absence of coupling or the presence of strong ferromagnetic interactions between the free layers (FL) can accelerate the switching process. In contrast, antiferromagnetic coupling may decelerate this process due to the complex dynamics of interlayer interactions. These findings, as shown in Fig. 2 and Fig. 3 for the configuration in Fig. 1(a) and in Fig. 4 and 5 for the setup in Fig. 1(b), underscore the intricate influence of IEC on magnetic switching, pointing out how device performance can be optimized by adjusting the coupling strengths.

This investigation into IEC's impact on STT-MRAM devices challenges conventional views on magnetic coupling, emphasizing the need for precision in engineering IEC to boost performance. The study suggests that optimal IEC tuning can lead to faster switching, increased device reliability, and improved data retention, marking a significant step forward in the field of spintronics and memory technology optimization.

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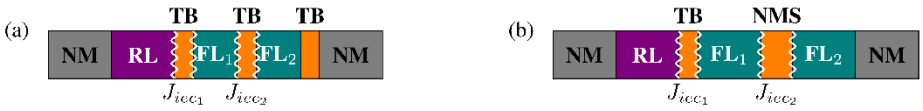

Figure 1: The intricate design of a multilayered MRAM cells in a more comprehensible form. (a) and (b) display a ultra-scaled MRAM cell. Color-coding is utilized for clear differentiation of components: the RL is marked in violet, the FL in teal, and the TB or NMS in orange. Non-magnetic (NM) contacts are represented in gray. Interfacial engineering regions are highlighted by white zigzag lines. The interaction strengths between the RL and the first FL (FL_1) and between FL_1 and the second FL (FL_2) are denoted by J_{iec_1} and J_{iec_2}, respectively.

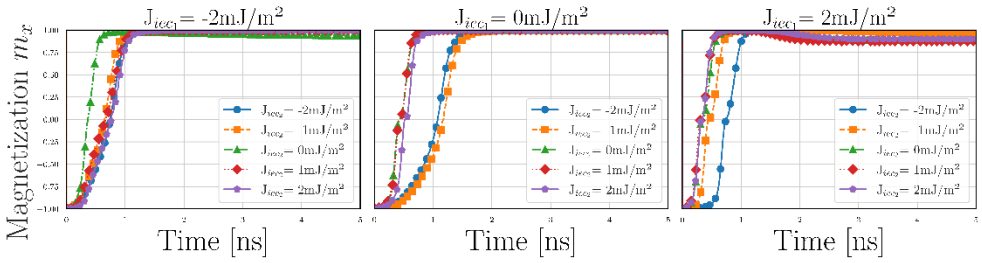

Figure 2: Magnetization dynamics for the multilayered MRAM cell in Fig. 1(a), with a particular emphasis on the influence of IEC strengths, J_{iec_1} and J_{iec_2}, on the switching processes from AP to P. The range of coupling strengths reflects experimental findings on magnetic interactions. The left panel sets J_{iec_1} to a negative value to demonstrate its effect on switching. The middle panel offers a contrast by setting J_{iec_1} to zero, while the right panel adopts a positive J_{iec_1}, each illustrating distinct dynamics. These simulations reveal the intricate and significant role of IEC in the switching behavior of advanced MRAM devices.

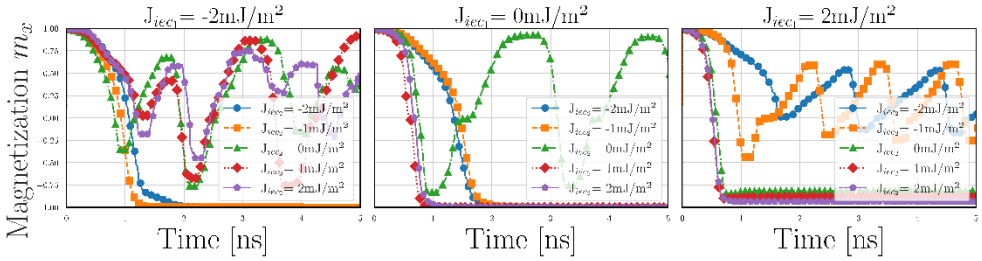

Figure 3: Magnetization dynamics during P to AP switching for the multilayer MRAM cell in Fig. 1(a), highlighting the critical role of IEC parameters, J_{iec_1} and J_{iec_2}.

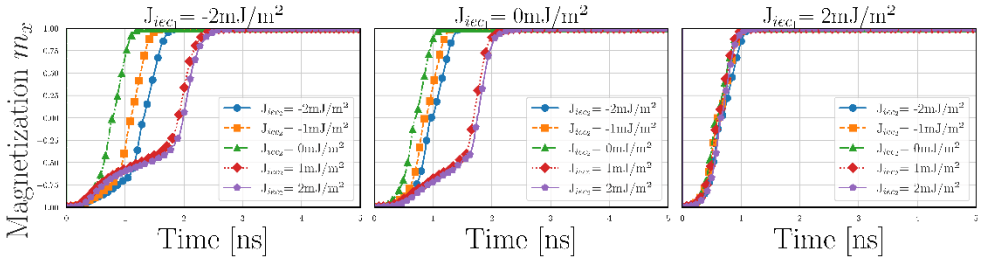

Figure 4: Magnetization dynamics during AP to P, for the multilayered MRAM cell in Fig. 1(b), highlighting the critical role of IEC parameters, J_{iec_1} and J_{iec_2}.

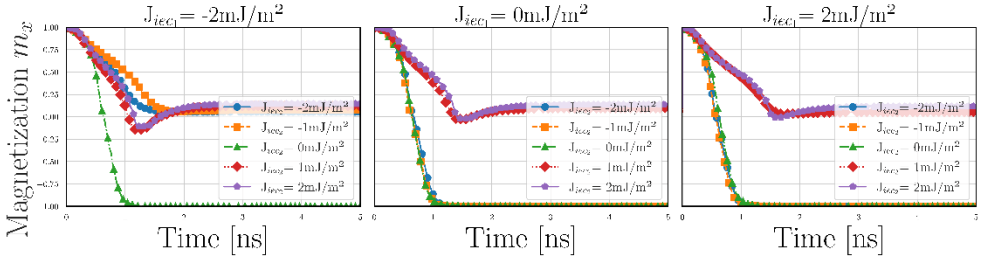

Figure 5: Magnetization dynamics during P to AP switching for the multilayer MRAM cell in Fig. 1(b), highlighting the critical role of IEC parameters, J_{iec_1} and J_{iec_2}.

Quantum Simulations of MoS_2 FETs Including Contact Effects

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2D materials have attracted considerable interest for applications in field-effect transistors (FETs) given their potential for high packing densities and excellent electrostatic control. Transition metal dichalcogenides (TMDs) have been extensively studied due to their promising electron transport properties down to monolayer thicknesses. MoS2 represents the most studied material in this class, with recent advances in its processing steadily bringing TMD-based technology closer to industrial applications [1]. One of the main challenges remains achieving low contact resistances due to Fermi level pinning at metal-TMD interfaces. Recently, the use of semimetals has been proposed to circumvent this issue. The combination of lower densities of states around the Fermi level and weaker interaction at semimetal-TMD interfaces results in contact resistances close to requirements for competing with Si technology [2]. The properties of semimetal-TMD interfaces have been studied using *ab-initio* simulations, providing insight into their electronic and charge transport characteristics [3]. However, such simulation frameworks are of limited use in device simulations due to their high computational cost. In this study we demonstrate a modelling approach that enables simulation of TMD-based devices with lengths of up to hundreds of nanometers with explicit descriptions of semimetal contacts.

In this work we simulate the electrical properties of field-effect transistors (FETs) based on monolayer (ML) MoS2 using a non-equilibrium Green's function (NEGF) solver [4]. Our approach enables computationally efficient simulations including quantum mechanical treatment of phonon scattering and electron tunneling phenomena. The electronic structure of Bi and ML-MoS2 are described by fitting atomistic simulations to continuum models based on k.p and the effective mass approximation. The properties of Bi/ML-MoS2 interfaces have been fitted to reproduce *ab-initio* simulations. Figure 1 illustrates simulated device geometries, where periodic boundary conditions have been applied along the width direction to simulate infinitely wide devices. Contact resistances have been extracted using the transmission line model. A back-gated architecture has been employed to emulate typical experimental setups for characterizing similar contact stacks.

Figure 2 shows the local density of states for a device in a state near its threshold voltage V_{TH}. Regions on either side of the channel explicitly describe source/drain junctions between semimetallic Bi and ML-MoS_2. Ohmic contacts between Bi and a metal are described via self-energies, as per the usual NEGF framework. Figure 3 shows the spectral current for the same state. As previously reported, inelastic phonon scattering is found to assist injection of carriers into ML-MoS2. Figure 4 shows the resistance across devices for gate lengths in the 20 nm – 50 nm range. A contact resistance of R_C=169 Ω.μm is extracted for a contact length L_C=10 nm and a channel carrier density of 10^{13} cm^{-2}, in good agreement with previous literature. Neglecting the effects of phonon scattering is found to increase contact resistance to R_C=390 Ω.μm, in excellent agreement with *ab-initio* simulations [3]. Figure 5 shows the contact resistance extracted for devices with varying contact lengths. R_C is

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observed to sharply increase for L_C < 15 nm, indicating a transfer length on the order of 10 nm. Figure 6 shows the transfer characteristics for a device with L_C=10 nm and L_{CH}=20 nm, where excellent switching characteristics are observed as the subthreshold swing remains at the thermodynamic limit. The simulation framework presented here is capable of capturing physical phenomena relevant for reproducing the electrical characteristics of Bi/ML-MoS2 contacts reported in experimental studies. Its low computational cost allows simulating length scales well-beyond that of atomistic frameworks and can be used to derive insight into device operation, opening an avenue for device and contact engineering in 2D materials using efficient quantum simulations.

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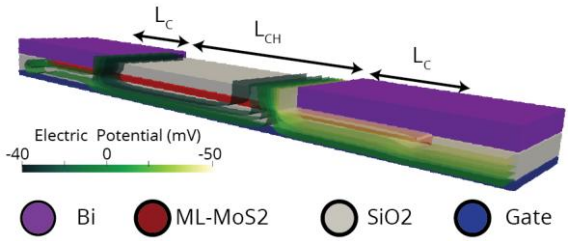

Figure 1: Simulated device geometry. L_C is the Bi/ML-MoS2 contact length, and L_{CH} the channel length. SiO2 thickness is 1 nm. Contour surfaces correspond to electric potential for V_{GS}≈V_{TH}.

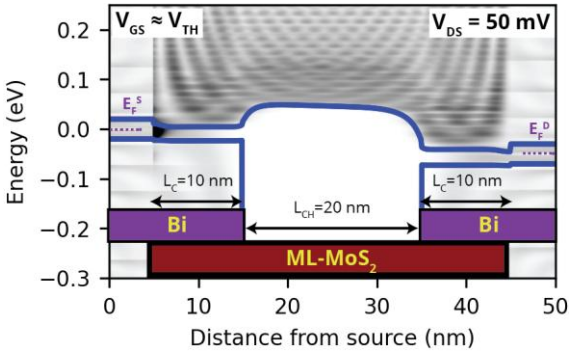

Figure 2: Local density of states. Coloured regions indicate active materials in each region.

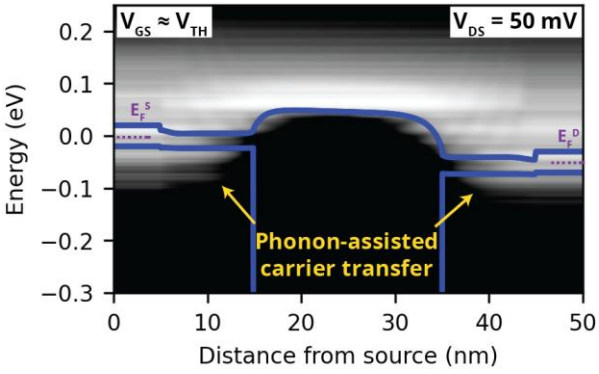

Figure 3: Spectral current. Brighter regions indicate higher current. L_C=10 nm and L_{CH} = 20 nm.

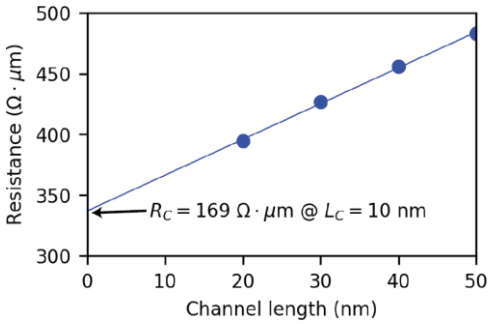

Figure 4: Contact resistance extracted using the transmission line model.

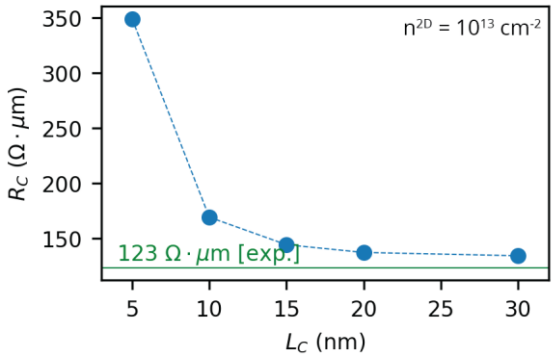

Figure 5: Contact resistance vs. contact length.

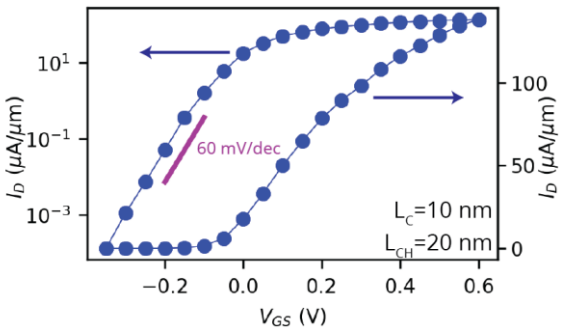

Figure 6: Device transfer characteristics.

Poster Presentation

TCAD Simulation of GAAFET for Cryogenic Temperature Operation to Achieve Low-Power and High-Performance Applications

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Abstract — In this work, we demonstrate the gate-all-around field-effect transistor (GAAFET) simulation at cryogenic temperature with a suitable low-threshold voltage (V_{th}) design to evaluate the characteristic enhancement from room temperature (T=300K) to T=77K. The cryogenic low-V_{th} design offers not only the scalability of the supply voltage (V_{dd}) but also the power-performance improvement of the ring oscillator (RO).

Index Terms – cryogenic temperature, GAAFET, high performance, low power, ring oscillator

Stacked GAAFET is a powerful candidate beyond 5-nm technology with superior electrostatics and short channel control [1]. The advanced technology node still suffers from the supply voltage scaling issue due to the V_{th} and static power constraints [2]. Cryogenic operation is one of the solutions to conquer the V_{dd} scaling issue because it shows the high I_{on}/I_{off} ratio due to the steep subthreshold swing (SS) and enhanced mobility [3]. Thus, we focus on the cryogenic characteristic of GAAFET and investigate the low-V_{th} design through work function engineering.

Fig. 1 demonstrates the TCAD simulation four-stacked GAAFET structure and the dimension parameters are based on the IRDS roadmap 2-nm technology node [4]. We set I_{off}=100 pA/μm as the low-V_{th} benchmark by tuning the gate work function at different temperatures. The device transfer and electrostatic characteristics are shown in Fig. 2 and Table I. The steep SS at 77K offers scalability of V_{th}, and the work function tuning increases I_{on} following the low-V_{th} benchmark. Therefore, the scaling V_{dd} is feasible by combining cryogenic operation and work function engineering in stacked GAAFET.

Three-stage GAAFET RO is established by TCAD mixed-mode device-circuit simulation as a benchmark circuit [5]. The transient behavior is illustrated in Fig. 3. Compared to the baseline (temperature=300K with V_{dd}=0.6V), the low-V_{th} design increases the on/off ratio and is beneficial to increase the RO frequency. In addition, reducing V_{dd} from 0.6V to 0.2V also reveals a higher operating frequency than the baseline shown in Table II, so it means the feasibility of scaling V_{dd} without sacrificing the speed.

In Fig. 4, we evaluate the dynamic power and operating frequency of the three-stage GAAFET RO. At the fixed dynamic power, the operating frequency is improved by about 236.1% at T=77K with V_{dd} reduction from 0.6V to 0.306V. Fig. 5 shows a notable enhancement in the frequency/dynamic power ratio because of decreased dynamic power and increased operating frequency. Consequently, this indicates that using the low-V_{th} design at cryogenic temperature enables high performance and low-power applications when not considering the cooling power.

Conclusion

The stacked GAAFET simulation shows better subthreshold characteristics at cryogenic temperature. The enhancement of I_{on} at low temperatures can be further improved by the work function engineering about three times following the low-V_{th} design. The three-stage GAAFET RO exhibits over twice the speed enhancement while maintaining constant dynamic power, achieved through a ~50% reduction in V_{dd} at T=77K. Additionally, the frequency/dynamic power ratio is significantly improved.

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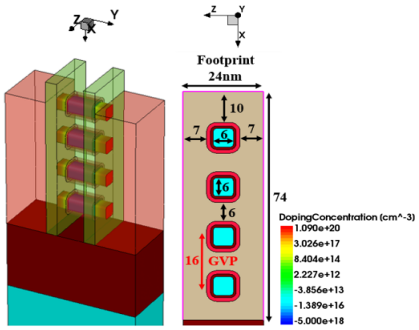

Fig. 1 GAAFET structure with parameters according to IRDS 2022 roadmap 2-nm technology node (G40M16/T2).

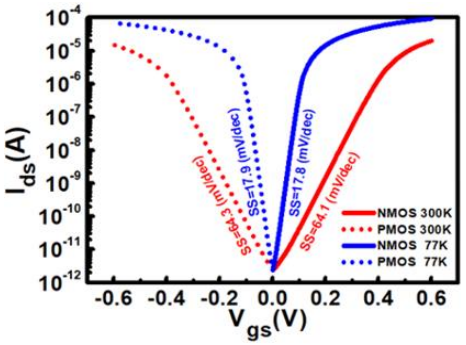

Fig. 2 Transfer curves of SOI GAAFET

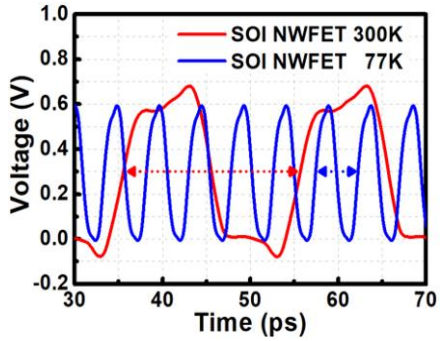

Fig. 3 The RO characteristics at 300K and 77K (with V_{dd}=0.6V)

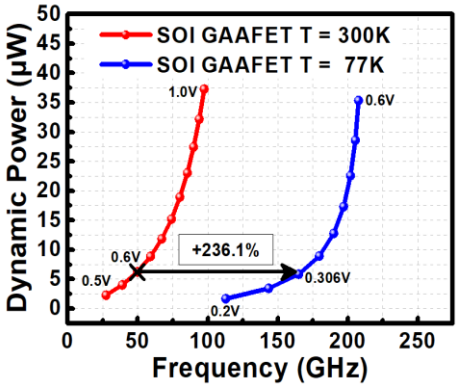

Fig. 4 Power and frequency curves of GAAFET at T=300K and T=77K with various V_{dd}.

Table I. The electrostatic characteristics of N/P GAAFET

	$I_{on,77K}/I_{on,300K}$	$V_{t\,300K}$ (V)	$V_{t\,77K}$ (V)	SS_{300K} (mV/dec)	SS_{77K} (mV/dec)
NFET	3.69	0.327	0.090	64.3	17.9
PFET	6.67	0.338	0.091	64.1	17.8

Table II. RO characteristics with various temperature and V_{dd}

T (K)	$\|V_{dd}\|$ (V)	Period (ps)	Frequency (GHz)
300	0.6	20.14	49.65
77	0.6	4.82	207.66
77	0.2	8.86	112.83

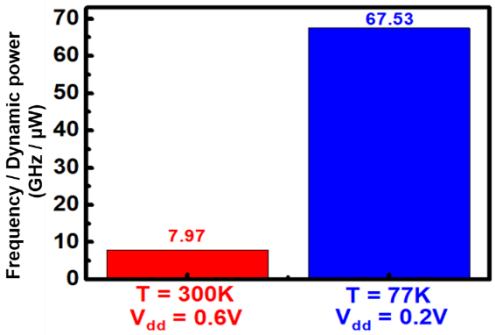

Fig. 5 Frequency/dynamic power ratio of GAAFET at T=300K with V_{dd}=0.6V and at T=77K with V_{dd}=0.2V

A Closed-Form Model for Gauss-Fermi Distribution in Amorphous and Organic Semiconductors

Elahe Rastegar Pashaki, Alexander Kloes, Ghader Darbandy

***Abstract*—In this paper, we introduce a closed-form model for the Gauss-Fermi integral, that can be used as the charge relation for disordered organic and amorphous semiconductors. A piecewise approximation of Fermi-Dirac distribution is considered, allowing us to solve the charge integral analytically. This analytical result supports both degenerate and non-degenerate conditions. then a parametric fitting function is suggested that represents the analytical results in a compact equation with a negligible error within a specific range of material parameters. The fitting function's values can be adjusted to support different material parameter ranges.**

***Index Terms*—Amorphous and organic semiconductors, Fermi-Dirac distribution, Gaussian DOS.**

I. Introduction

IT has been shown that the effective mobility of organic material can be better described by considering the Gaussian density of states (DOS) for charge distribution [1]. Finding the corresponding charge densities to this Gaussian DOS with the Boltzmann approximation was the main subject of our previous work in [2]. However, the non-degenerate condition becomes more fragile by increasing the disorder factor in organic and amorphous semiconductors [3], [4], and considering the Fermi-Dirac distribution can provide a more general description of these devices. Since the charge integral has no analytical solution with Fermi-Dirac distribution, it is necessary to define approximations. In Ref. [4], the charge integral is solved analytically by considering $T \to \infty$ and $T \to 0$, that correspond to non-degenerate and degenerate conditions, respectively. Thus, the final result is a conditional relation that has to choose between two equations. However, the approximation of this work supports the complete form of Fermi-Dirac function in a wide temperature range and provides a general description that supports the degenerate and non-degenerate conditions in one equation. Although the derived analytical solution is a big relation, at the next step we used it's results to propose a parametric closed-form function that represents the analytical behaviour within a range of material parameters with negligible error. This final equation can be used in the compact modeling of amorphous and organic transistors.

II. Band diagram

Fig. 1 shows the Gaussian DOS and provides a detailed energy diagram of the organic semiconductors. In this diagram,

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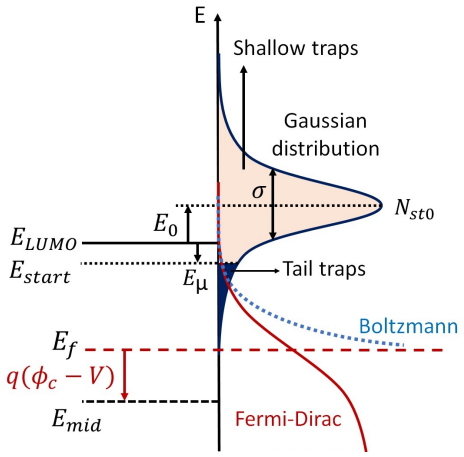

Figure 1. Gaussian density of states and the detailed energy diagram of the organic semiconductor.

E_μ represents the distance of E_{start} relative to the LUMO (Least Unoccupied Molecular Orbital), at which charge carriers start to behave as quasi-mobile charges. A positive value for E_μ means this energy level lies below the LUMO. The filling probability of this Gaussian profile is according to the Fermi-Dirac distribution that links with the chemical potential. The Φ_c parameter represents the midgap potential and corresponds to the distance of the Fermi level (E_f) from the midgap (E_{mid}). The potential Φ_c is positive when E_f is above E_{mid}. This schematic provides a useful vision of the more probable degeneracy condition in disordered semiconductors. By increasing the disorder factor (σ), the DOS profile extends to the bandgap of the semiconductor [5], and the Boltzmann approximation could make a considerable error in this region, that grows by further shifting the midgap potential due to an applied voltage (V).

III. Charge integral

First, the Fermi-Dirac equation is approximated with a set of simple piecewise functions that allow us to analytically solve the charge integral with the Gaussian DOS.

$$f(E) \approx \begin{cases} 1 - \exp\left(\frac{E-E_f}{\mathrm{kT}}\right) & -\infty < E-E_f < \frac{-5\mathrm{kT}}{2} \\ 1 - \left(\frac{E-E_f+4.1\mathrm{kT}}{6\mathrm{kT}}\right)^2 & \frac{-5\mathrm{kT}}{2} < E-E_f < \frac{-\mathrm{kT}}{2} \\ 0.5 - \frac{E-E_f}{4\mathrm{kT}} & \frac{-\mathrm{kT}}{2} < E-E_f < \frac{+\mathrm{kT}}{2} \\ \left(\frac{E-E_f-4.1\mathrm{kT}}{6\mathrm{kT}}\right)^2 & \frac{+\mathrm{kT}}{2} < E-E_f < \frac{+5\mathrm{kT}}{2} \\ \exp\left(-\frac{E-E_f}{\mathrm{kT}}\right) & \frac{+5\mathrm{kT}}{2} < E-E_f < +\infty \end{cases} \quad (1)$$

where kT is the thermal energy. The Gaussian distribution is considered as follows:

$$\Gamma(E) = \frac{N_{st0}}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(E - E_{LUMO} - E_0)^2}{2\sigma^2}\right) \quad (2)$$

where N_{st0} is the peak value, and σ is the standard deviation (disorder factor) of the Gaussian DOS. The center of this Gaussian distribution lies at $E_{LUMO}+E_0$, where E_0 controls the distance of the center from LUMO level.

The charge density is $Q' = qd_m \int \Gamma(E) \cdot f(E) dE$, where d_m is the thickness of accumulated charge layer in the channel. Using Eq. (1), Eq. (2), the charge integral has a complex analytical solution that barely can be considered as a compact model. However, we will propose a parametric and compact function to the charge density as an approximation of this exact analytical solution that reduces the calculation complexity. The final result is:

$$\frac{Q'_{total}}{Q'_m} = \frac{F_{min} \exp\left(F_s \frac{(q(\Phi_c - V) - F_c)}{\mathrm{kT}}\right) + F_{max}}{\exp\left(F_s \frac{(q(\Phi_c - V) - F_c)}{\mathrm{kT}}\right) + 1} \quad (3)$$

where F_{min}, F_{max}, F_s, and F_c are material dependent and fixed fitting parameters, defined as follows:

$$F_{min} = \frac{Q'_{total}}{Q'_m}|_{E_F = E_{LUMO}} \quad (4)$$

$$F_{max} = \frac{Q'_{total}}{Q'_m}|_{\text{Boltzmann}} = \frac{2}{1 - \mathrm{erf}\,(\Sigma - \mathrm{R_m})}$$

$$F_c = \frac{\mathrm{E_G}}{2}\left[\frac{5\mathrm{E_0}}{4} + \left(0.92 + 0.6\mathrm{E_G} - 12\sigma - 0.59\mathrm{E_G^2} + 14.2\sigma\mathrm{E_G} - 96\sigma^2 + 0.15\mathrm{E_G^3} - 3.9\sigma\mathrm{E_G^2} + 27\sigma^2\mathrm{E_G} + 3.333\sigma^3\right) - \left(5.542\times10^{-6}\mathrm{T^2} - 4.962\times10^{-3}\mathrm{T} + 0.9893\right)\right]$$

$$F_s = \frac{2}{E_G}|F_c|^{\,5.371F_c^2 - 0.4534F_c + 6\sigma}$$

where $\Sigma \doteq \sigma/(\sqrt{2}\mathrm{kT})$, $\mathrm{R_m} \doteq (\mathrm{E_0} + \mathrm{E_\mu})/(\sqrt{2}\sigma)$. The F_c and F_s in Eq. (4) are just fitted numerically and don't have any physical meaning. E_G ,E_0, E_μ, and σ are in eV, T is in K, and all fitted numbers are supposed to compensate the dimensions of physical parameters to finally make F_c in eV and F_s a unit-less parameter. The F_{min} is determined by using the main analytical relations for Q'_{total}(total) and Q'_m (shallow traps) at $E_f = E_{LUMO}$. Therefore, like as other parameters, it is a bias-independent fixed number that only needs one-time calculation. It should be mentioned that the error of this fitting function is not uniform for all possible parameter sets, but coefficients in F_c and F_s are chosen to create an appropriate fitting in the parameter range of Tab. (I), which are applicable ranges based on reported values in [6], [7]. The suggested equation can be adapted to various parameter ranges by discovering new fitting functions for F_c and F_s (representing the center and slope of Q'_{total}/Q'_m).

The result of Eq. (3) is shown in Fig. 2 for two sets of parameters, and as can be seen, there is a good agreement between the exact analytical results and the proposed compact model within the valid range.

Table I
VALID PARAMETER RANGE FOR DEFINED F_c AND F_s IN EQ. (4)

	min	max
E_G	$1.1\,eV$	$2.5\,eV$
E_0	$-0.3\,eV$	$0.1\,eV$
E_μ	$-0.2\,eV$	$0.4\,eV$
σ	$0.07\,eV$ $(\approx 3kT)$	$0.13\,eV$ $(\approx 6kT)$

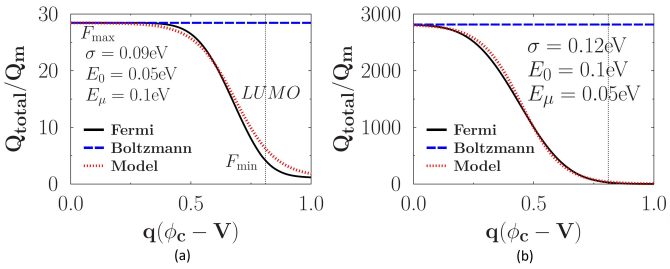

Figure 2. Q'_{total}/Q'_m plot with the Boltzmann, Fermi Dirac, and the closed-form model result for $T = 300\,K$, $E_G = 1.63\,eV$, (a) $E_0 = 0.05\,eV$, $E_\mu = 0.1\,eV$, $\sigma = 0.09\,eV$ and (b) $E_0 = 0.1\,eV$, $E_\mu = 0.05\,eV$, $\sigma = 0.12\,eV$.

Finally, the mobile charge density can be determined by Eq. (3) and Q'_{total}, which is approximated as follows:

$$Q'_{total} = \frac{qN_{st0} \cdot d_m}{2} \cdot \left\{\exp\left(\Sigma^2 - 2\Delta\Sigma\right) \cdot \left[1 - \mathrm{erf}\,(\Sigma - \Delta)\right] \left[\exp\left(2\Delta\Sigma + \Sigma^2\right) \cdot \left(\mathrm{erf}\,(\Delta + \Sigma) - 1\right) + \mathrm{erf}\,(-\Delta) + 1\right]\right\} \quad (5)$$

where $\Delta \doteq (\mathrm{E_{LUMO}} + \mathrm{E_0} - \mathrm{E_f})/\left(\sqrt{2}\sigma\right)$.

IV. Conclusion

We proposed an analytical solution for the Q'_{total} to Q'_m ratio with Gauss-Fermi distribution, then derived a closed-form and compact equation for this ratio. This solution separates fixed physical parameters from bias-dependent variables, leading to a reduction in computational complexity while ensuring accuracy within an acceptable range. This simple equation supports both degenerate and non-degenerate conditions in a single relation and can be applied to a range of disordered organic and amorphous semiconductors.

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Boosting the Capacity of Driving the Drain Current of the FinFET by a Simple Changing of the CMOS ICs Manufacturing Process

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This work proposes a simple change of the channel CMOS ICs manufacturing processes to manufacture FinFETs, focusing on boosting their capacity to drive electrical current concerning the Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) manufacturing process [1-2]. Called "Gate in Diagonal-FinFET" (GiD-FinFET), it was carefully designed so its gate region is non-orthogonal to the Fin, as is observed in the Gate Conventional-FinFET counterpart (GC-FinFET). Three-dimensional (3D) numerical simulations were done using the Atlas Semiconductor Devices Simulator from Silvaco Co. to quantify the influence of the angle between the gate and Fin regions in the drain to source current, compared to the one observed in the conventional FinFET counterpart, considering that these devices present the same gate area. Figure 1 illustrates the simplified 3D structures of a conventional FinFET (Figure 1.a: "+" mode) and a proposed GiD-FinFET (Figure 1.b: "x" mode), where β is the angle defined by the crossing between the gate and Fin regions of the FinFET, and in this work, it was considered equal to 45º, H_{Fin} (=60 nm) are the Fins' heights of the conventional FinFET and GiD-FinFET, which it defines the FinFET's channel width (W_{FinFET}=2.H_{Fin}), however it define the pseudo-height of the GiD-FinFET (H_{Fin}'), that can be calculated as a function of H_{Fin} [H'_{Fin}=H_{Fin}/sin(β): 84,9 nm for β=45º], that also defines its channel width ($W_{GiD\text{-}FinFET}$=2.H_{Fin}'), L_g (=65 nm) is the channel length and W_{Fin} (=20 nm) is the Fin width. Besides, we consider the impurities concentrations of acceptors (N_A) and donors (N_D) of 1.10^{15} cm^{-3} and 5.10^{20} cm^{-3}, respectively, the gate thin oxide thickness (t_{ox}) is equal to 2 nm, and the buried oxide thickness (t_{box}) is equal to 140 nm. To manufacture a GiD-FinFET, it is only necessary to incline, with a specific θ angle, that is equal to 90-β, the wafer after the manufacturing processes that define the Fin of FinFET (Figure 2). Afterwards, the same CMOS ICs manufacturing processes must be processed (Gate formation, Deposition and Etching of the Insulator Layer, Source and Drain Formation, Connections and Finalization) to build a GiD-FinFET [3].

Figures 3 and 4 illustrate the 3D structures of the conventional FinFET and GiD-FinFET, respectively, implemented using the DevEdi3D of Silvaco Co., which were used to perform the 3D numerical simulations. The threshold voltages (V_{TH}) of these FinFETs are equal to 390 mV, which were obtained concerning a drain-to-source voltage (V_{DS}) of 50 mV [4]. Figures 4 and 5 illustrate the drain-to-source current (I_{DS}) as a function of the gate-to-source voltage (V_{GS}), for drain-to-source voltage (V_{DS}) equal to 0.5 V and I_{DS} as a function of V_{DS}, for V_{GS} equal to 1.2 V, respectively, of the FinFETs considered in this work, regarding that they present the same geometric dimensions of the Fins. Based on Figures 4 and 5, we observe that the GiD-FinFETs I_{DS} with a β equal to 45º are 32% (for V_{DS} equal to 0.5 V) and 33% (V_{GS} equal to 1.5V), respectively, higher than those observed in the conventional FinFET counterpart. This can be justified mainly because the effective channel width of the GiD-FinFETs is 41.3% larger than that observed in the conventional FinFET counterpart, which leads to better use of its Fin region for the conducting I_{DS} in relation to the one measured in the conventional

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FinFET. Therefore, based on these results, by changing the β between the gate and Fin regions, we can boost the FinFETs I_{DS} and consequently their abilities to buffer electrical current, aiming the reduction of the number of Fins that must be put in parallel to define a specific I_{DS} and their occupied die areas.

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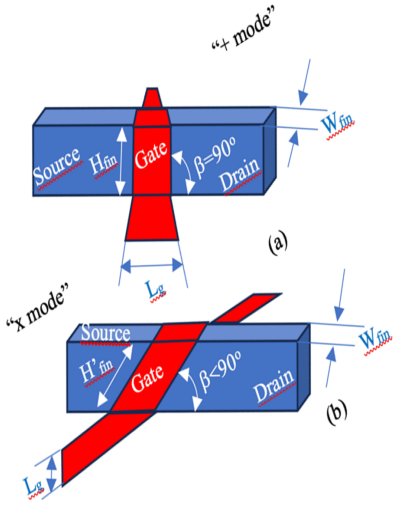

Figure 1. Simplified 3D of a FinFET and a GiD-FinFET

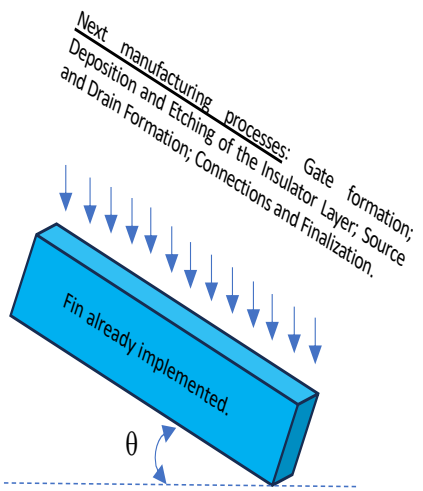

Figure 2. "θ" inclination of the of the conventional FinFET

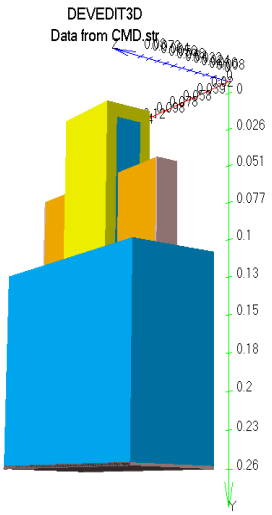

Figure 3. The 3D structure of FinFET (DevEdit3D)

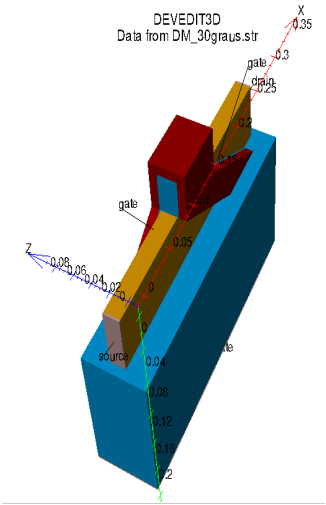

Figure 4. The 3D structure of GiD-FinFET (DevEdit3d)

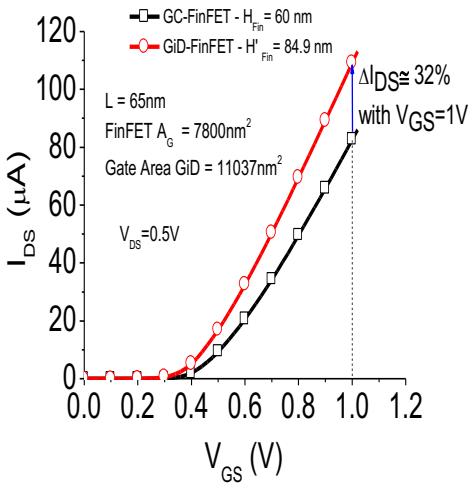

Figure 5. I_{DS} as a function of V_{GS}, for V_{DS}=0.5V

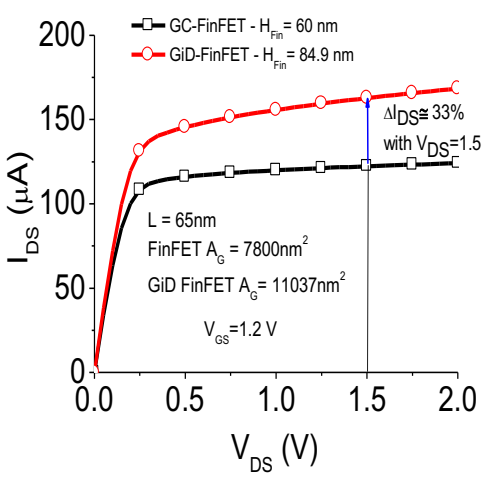

Figure 5. I_{DS} as a function of V_{GS}, for V_{GS} of 1.2 V.

Resistive switching mechanisms in RRAM memory structures based on copper (II) oxide

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Among emerging technologies, one of the most promising memory devices is resistive random access memory (RRAM). It holds significant promise due to its durability, fast switching speed, and ease of manufacturing. RRAM employs a straightforward design featuring a dielectric thin layer sandwiched between two electrodes. The ability to write and read data is attributed to the memristor effect - a phenomenon wherein the electrical resistance of a dielectric material changes between a high resistance state (HRS) and a low resistance state (LRS) due to physical processes activated by an external electric field. This process involves complex interactions and modifications at the atomic or molecular level, resulting in a dynamic change in the material's resistance. A deeper understanding of these mechanisms is critical to achieving an optimal design for memory structures, thus enhancing overall efficiency and reliability. Despite notable progress and successful demonstrations of RRAM technology, the complex physics governing resistive switching remains incompletely understood.

The presented research concerns the phenomenon of resistive switching in structures based on copper (II) oxide grown from an aqueous solution through an innovative hydrothermal method [1]. This approach is characterized by mild growth conditions (temperature does not exceed 100°C and in atmospheric pressure), allowing synthesis in an open system. It also features an ultra-fast growth rate (lasting from several seconds to 6 minutes) and avoids the use of toxic substances, making the growth technology environmentally friendly. Previous studies revealed organic compound contamination in as-grown layers. Thus, a procedure of cyclically repeating the hydrothermal growth process and rapid thermal annealing (HT+RTA) was implemented to obtain continuous, electrically stable layers with reduced content of these impurities. The phenomenon of resistive switching is observed for both as grown and ‘HT+RTA’ layers. Devices fabricated with 'HT + RTP' films exhibit improved stability and repeatability of resistive switching characteristics (fig.2) compared to those with as-grown layers, maintaining good retention of low resistance state (LRS) and high resistance state (HRS). Additionally, the memory window obtained for the RRAM structure with 'HT + RTP' layers demonstrates durable stability, as indicated by a high HRS/LRS ratio approximated to ten years [2].

Two main resistive switching mechanisms are discussed in the literature [3]. One proposes that switching occurs due to charge trapping in the active layer or its interface with the electrode. The second mechanism, common in RRAM structures based on metal oxides, involves the forming and disrupting of conductive filaments through ion migration within the active layer. Investigation carried out using tunneling AFM has shown that such processes serve as a basis for resistive switching in examined structures based on CuO films. The ongoing research also includes investigating the mechanisms of carrier transport within these structures. Voltage dependency analysis was conducted using the I~f(V) relationships outlined in [3]. An important finding is that the ln(I)~ln(V) characteristics exhibit linearity

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across almost the entire range of tested voltages. This observation strongly suggests that the space charge limited current (SCLC) is the predominant conduction mechanism in these particular memristor structures. Further analysis of the slopes of the curves when plotted on a logarithmic scale (ln(I) vs. ln(V)) (fig.3), along with comparison to model values for SCLC, provides additional validation of this conclusion. Minor deviations from the model slope values result from the co-occurrence of other mechanisms within specific voltage ranges, which is still under investigation.

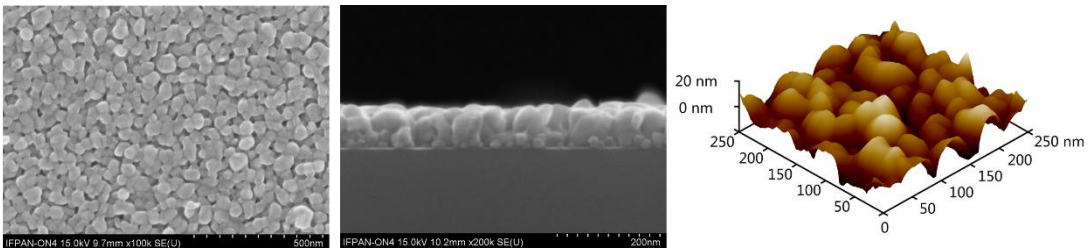

Fig. 1. SEM and AFM images of CuO films ('HT+RTA') used as an active layer in examined RRAM structures.

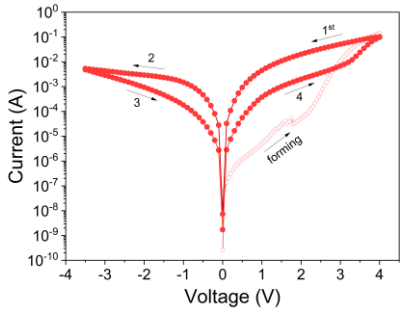

Fig. 2. I-V characteristics for Al/Si(n^{+++})/CuO/Au structure indicating the occurrence of the memristive effect.

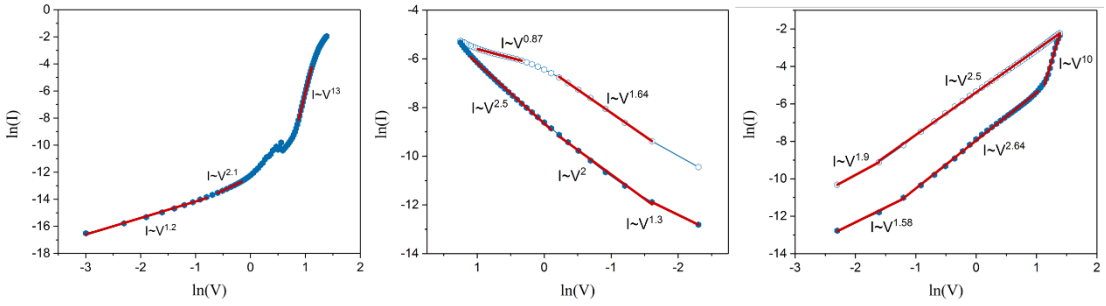

Fig. 3. I-V data presented in the ln(I) vs. ln(V) coordinate system corresponding to the SCLC mechanism, with indicated slope values, respectively for the formation curve, V<0 and V>0.

Acknowledges

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Investigation and Modeling Thermoelectric Performance of Multilayered Sb-rich GeSbTe Phase Change Memory Using Finite Element Method

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Abstract

This study introduces a novel finite-element method (FEM)-based thermoelectric model designed to precisely characterize the RESET operation of phase-change memory (PCM) devices with and without Antimony (Sb)-rich multilayered Ge2Sb2Te5 (GST) as the phase-change material. PCM stands out as a promising candidate for future non-volatile memory technologies due to its scalability, reliability, endurance, and multi-level cell (MLC) storage capabilities. It is a leading technology among new non-volatile memories (NVM), offering a solid alternative to flash technology. It has been presented as Storage Class Memory (SCM) alternative recently thanks to its competitive properties [1]. Changing market trends toward low power applications create opportunities for emerging NVMs [2]. Through detailed analysis using COMSOL Multiphysics, we used heat transfer equations to include the additional thermoelectric heating components arising from the Joule heating within the materials.

Our model implements both resistive Joule heating and thermoelectric phenomena, which are crucial in smaller devices due to enhanced thermal confinement. The model utilizes field and temperature-dependent material parameters and physical properties for the crystalline and amorphous phases of GST [3], providing a more accurate representation of the device characteristics. Our findings are in good correlation with experimental studies, with particular emphasis on the temperature-dependent operation characteristics of the devices [4]. This work will help in advancing our understanding of PCM device operation, and to the optimization of device design for enhanced efficiency in memory storage applications.

Simulation and modeling studies have proceeded to determine the thermal and electrical attributes of PCM materials for different geometries using projected parameters. The focus of these studies is to establish the thermal and electrical characteristics of PCM materials, for a specific multilayered geometry, using predicted parameters. We anticipate that these simulation studies will reveal significant insights into the thermo-electric performance of these materials. In this study, we turned our attention to a new geometry of GST phase change memory. This design features a multi-layered Sb-Rich “J” type heater structure. Our analysis of temperature distribution and phase change behavior have revealed that a 1 V pulse with a 10 ns pulse width is highly effective in creating a balanced amorphous section in close proximity to the heater contact. Comparing this result with conventional GST section without Sb layers provides new possibilities and progress towards a system not only demanding lower power consumption but also a much faster RESET operation.

Aknowledgment

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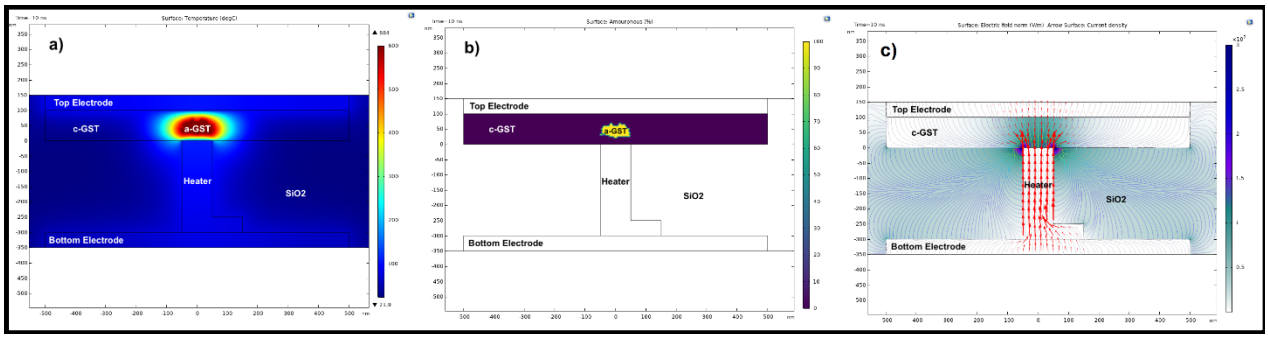

Figure 1. a) Temperature distribution b) Phase change c) Electric field and current density after 1 V – 10 ns pulse width RESET pulse on "J" structure GST.

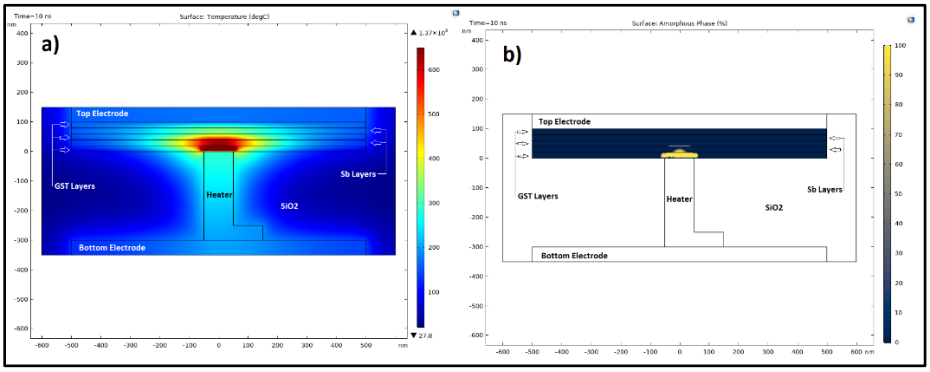

Figure 2. a) Temperature distribution b) Phase change c) Electric field and current density after 1 V – 10 ns pulse width RESET pulse on Multi-layered Sb-Rich "J" structure GST.

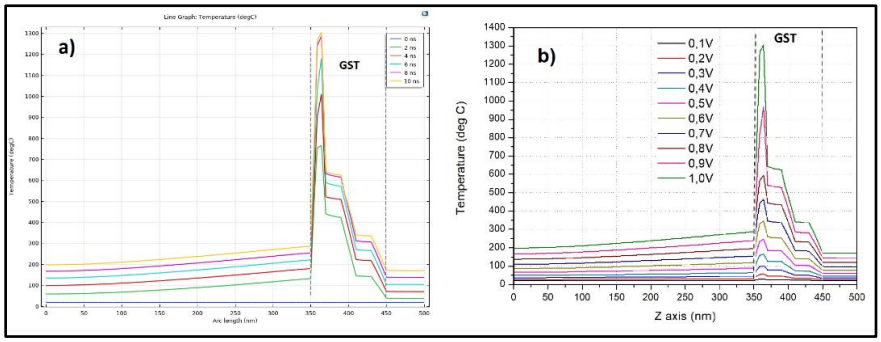

Figure 3. a) Temperature evolution during 1 V – 10 ns pulse and b) Reached temperature levels after 0 V to 1 V – 10 ns pulse width RESET operation on Multi-layered Sb-Rich "J" structure GST.

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Temperature Resilient 1-T FDSOI Neuron for Reliable Neuromorphic Computing

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Abstract

This work investigates temperature effects on Fully Depleted Silicon on Insulator (FDSOI) MOSFET based single transistor neuron for neuromorphic computing. This was performed by analyzing the spiking frequency response, energy per spike and latch voltage outputs for FDSOI MOSFET as a function of temperature. Results have shown that the FDSOI MOSFET provides stable performance with temperatures varying from 300K up to 380K for large negative gate bias i.e., -1 V. A single transistor latch (STL) function is enabled via thermally insensitive band-to-band tunneling (BTBT), an alternative to the thermally sensitive Impact Ionization (II). This results in temperature resilient thermally stable neuronal operation.

Keywords: Neuromorphic computing, single-transistor neuron, FDSOI MOSFET, thermally stable.

I. Introduction

Nowadays, non-volatile memory (NVM)-based neuromorphic computing is showing remarkable success. Many studies have been conducted on resistive random access memory (RRAM) [1], one type of promising NVM, to elucidate the reliability requirements for neuromorphic application. A lot of research has recently been done on hardware-based neuromorphic systems in an attempt to get around the drawbacks of the von Neumann architecture, which creates a bottleneck between the processor and memory. Spiking neural networks (SNNs) require artificial neuron devices that perform the leaky- integrate-and-fire (LIF) behaviour [2]. Specifically, the STL is used to simulate neuronal firing in MOSFETs. But, since the II rate is influenced by temperature, the STL becomes temperature-sensitive when the single transistor neuron is activated. It may be difficult to do trustworthy computing with such thermal instability. And, without an extra temperature control module, which usually takes up a lot of space, controlling temperature is challenging. The severity of this issue increases when neuromorphic hardware is used with significant temperature swings, like in autonomous cars, airplanes, and IOT sensors, etc. [5].

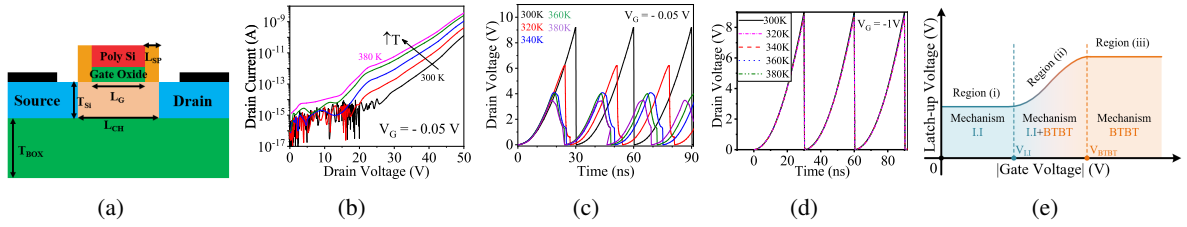
II. Device structure and Operation

Here, we show that a thermally steady FDSOI STL neuron by controlling a negative V_G. The schematic representation of FDSOI MOSFET with 100 nm channel length (L_{CH}) and 20 nm channel thickness (T_{Si}) is shown in Fig. 1(a). The device is simulated with the help of well calibrated Sentaurus TCAD [7]. The FDSOI LIF neuron exhibits the spiking behaviour without any reset circuitry by using the STL phenomena. When a constant drain current is given at the drain terminal with -V_G, the accumulation of charges will develop the potential at drain electrode (V_D) over the time. If V_D reaches certain threshold (V_{Latch}), the channel will allow the current flow and device will change from high resistance state (HRS) to low resistance state (LRS), which will mimic the spiking behaviour of neuron with respect to time [6]. It can be used for neuromorphic computing application. However, the temperature reliability of neuron is one of the important parameter to be analyzed. This work makes an attempt to establish a thermally stable single transistor neuron which will avoid any additional circuitry as well as ensure reliable computing paradigm.

III. Results and discussion

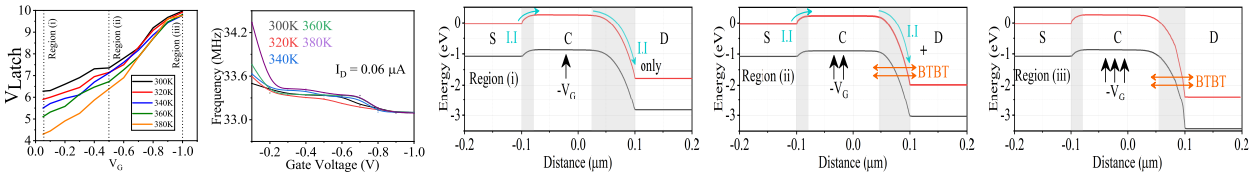
A significant amount of current flows over the STL instantaneously when V_D reaches a specific i.e, V_{Latch}, as illustrated in Fig. 1(b). The temperature variation in STL affects the V_{Latch} in I_D-V_D characteristics for -V_G. The temperature inducing II and followed by a positive feedback [8]. After V_D reaches V_{Latch}, the device allow high current flow by changing the HRS to LRS, referred as STL. It is utilized for mimicking of integration and firing behaviour of LIF neuron. Fig. 1 shows the transient behaviour of STL neuron. The developed drain potential over the time for different temperature is estimated at V_G = -0.05 V as shown in Fig. 1(c). It is observed that the spiking characteristics of STL neuron are sensitive to temperature, since the II is directly related to the temperature. However, by carefully adjusting the V_G at a particular bias (in this case at -1 V), we can able to make it temperature insensitive V_{Latch} as depicted in Fig. 1(d).

On the other hand, if BTBT mechanism is used for triggering the STL, the spiking frequency of the STL neuron is observed to be stable, independent of temperature. It is noted that the BTBT mechanism exhibits temperature in-variance. A pictorial representation of both II and BTBT mechanisms used by V_G to control the STL is shown in Fig. 1(e). Considering V_{II} and V_{BTBT} as the two criteria, V_G is divided into three regions. A V_G less than -0.5 V is considered as a region for II,



(a) (b) (c) (d) (e)

Fig. 1. (a) Output characteristics of the FDSOI MOSFET with negative V_G which shows the STL behaviour; Mimicking of spiking behaviour at (b) V_G = -0.05 V, (c) V_G = -1 V, with different temperatures (d) Graphical representation of three regions w.r.t. -V_G



(a) (b) (c) (d) (e)

Fig. 2. (a) Dependence of temperature on V_G vs V_{Latch} (b) Frequency of spiking with temperature variation for different gate biases (c) Region (i) only with II, (d) Region (ii) with both II and BTBT (e) Region (iii) with BTBT

which is noted as V_{II}. At this region, II is dominant and primary reason for STL phenomena. The region where BTBT controls the STL behavior is V_G exceeding -1 V, i.e, V_{BTBT}. BTBT and II are both involved in controlling the V_{Latch} between -0.5 V and -1 V. The transition of V_{Latch} from region to region is described in Fig. 2(a). Similarly, the frequency of spiking sensitive to the temperature for different V_G are observed in Fig. 2(b) and the resilient behavior can be observed at V_G=-1 V. . Fig. 2 (c) shows the II mechanism, which allows the generation of e-h pairs at the drain-channel junction to trigger the STL with increased temperature for the range V_G up to -0.5 V. When V_G is more negative beyond -0.5 V, the band overlapping is observed more compared to V_G less than -0.5 V. Hence, it is observed that the dominance of temperature sensitive II is reduced for the control of STL behaviour and BTBT is introduced, which is insensitive to temperature as shown in Fig. 2(d). As illustrated in Fig. 2(e), when V_G= -1 V, BTBT mechanism is dominant. It should be mentioned that because of the large potential difference between the body and drain, the holes created by BTBT are stored in the floating body [9] to cause the STL.

Because BTBT is temperature-immune, the STL and spiking characteristics are thus thermally stable in region (iii). It is observed that at higher negative V_G values, BTBT is more dominant, while II. is more dominant at lower negative V_G values. It is possible to achieve robust and thermally stable neuromorphic operation during temperature changes by using BTBT to control V_G and initiate neuronal spiking.

IV. Conclusion

In summary, a thermally stable FDSOI based 1T-nueron is demonstrated. Two methods were available for generating holes in a floating body: BTBT and II. The firing and resting characteristics of neurons become thermally stable if the temperature sensitive II led activation mechanism is substituted with the temperature-insensitive BTBT one. To confirm this, the spiking frequency is observed and concluded a temperature resilient behavior at V_G=-1 V.

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TCAD Simulations of Single Event Effects in Quasi-vertical GaN Schottky Barrier Diodes with Guard Rings for Space Applications

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Gallium nitride (GaN) devices have attracted significant interest in the space industry due to their potential for superior radiation tolerance [1-3]. The natural radiation environment comprises of particles of various nature and energy. Single event effects (SEEs) are one of the most detrimental mechanisms, which could render GaN Schottky Barrier Diodes (SBDs) non-operational in space systems. There are recent Technology Computer Aided Design (TCAD) simulation studies that evaluate SEEs [2] and single event burnout hardening on GaN transistors with double field plates [3]. Chen *et al*. [4] have recently reported TCAD simulations of SiC Schottky diodes with multiple buffer layers for space power conversion. To the best of the authors' knowledge, no radiation immunity studies have been reported for GaN SBDs. The objective of this paper is to provide design guidelines for improved radiation immunity of quasi-vertical GaN SBDs by using single or multiple p-GaN guard rings.

Figure 1(a) shows a GaN SBD device cross-section without guard rings, that have been previously fabricated [5]. To investigate the impact of heavy-ion strike on this device, a single event effect model was included in the TCAD simulation. The mechanism of SEE is depicted in Fig. 1(a). As ions traverse the device, a substantial generation of electron-hole pairs occurs, contributing to a parasitic current that can cause permanent damage. Hence the guard ring structure is proposed as shown in Fig. 1(b). The device parameters used in the simulations are summarized in Table I. The accuracy of the model is tested on experimental current-voltage (I-V) data [5] for a GaN SBD without the guard rings. There is good agreement between experimental and simulated I-V curves as shown in Figure 2(a). The transient current of an SBD without a guard ring rises sharply in Fig. 2(b). In contrast, the SBDs with guard rings exhibit a lower transient current, which further decreases steadily with increasing p-type carrier concentration of guard ring from 10^{17} cm^{-3} to 10^{19} cm^{-3} (Fig. 2(b)). Figures 2(c) and (d) depict transient current and electric field distribution, while Figs. 3(a)-(b) electron distribution for GaN SBDs with single and multiple guard rings using the highest carrier concentration of p-GaN of 10^{19} cm^{-3}. It is evident from Figures 3(a) and (b) that multiple guard rings induce a larger depletion region that hinders electron drift, causing the decrease in transient current and hence effectively enhancing radiation immunity due to the uniform distribution of the electric field. In summary, this work provides design guideline to enhance SEE immunity of GaN SBDs for space applications.

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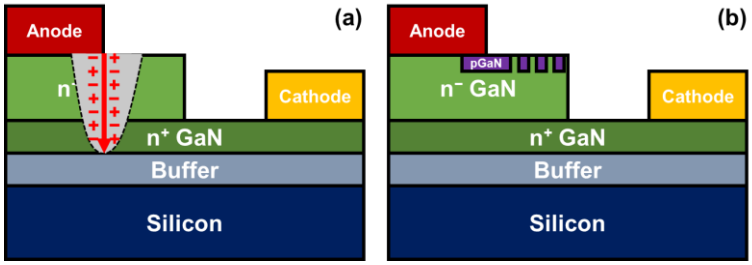

Table I. A summary of device parameters used in simulations.

Parameters	Values
n^- GaN doping/thickness	1×10^{15} cm^{-3} / 2 μm
n^+ GaN doping/thickness	1×10^{17} cm^{-3} / 1 μm
p-GaN doping/thickness	1×10^{19} cm^{-3} / 0.2 μm
p-GaN width (single/multiple)	10 μm / 2 μm
p-GaN spacing	1 μm
Incident ion energy	0.6 pC/μm

Fig. 1 GaN SBD cross-sections: (a) illustrating SEE; (b) with p-GaN rings.

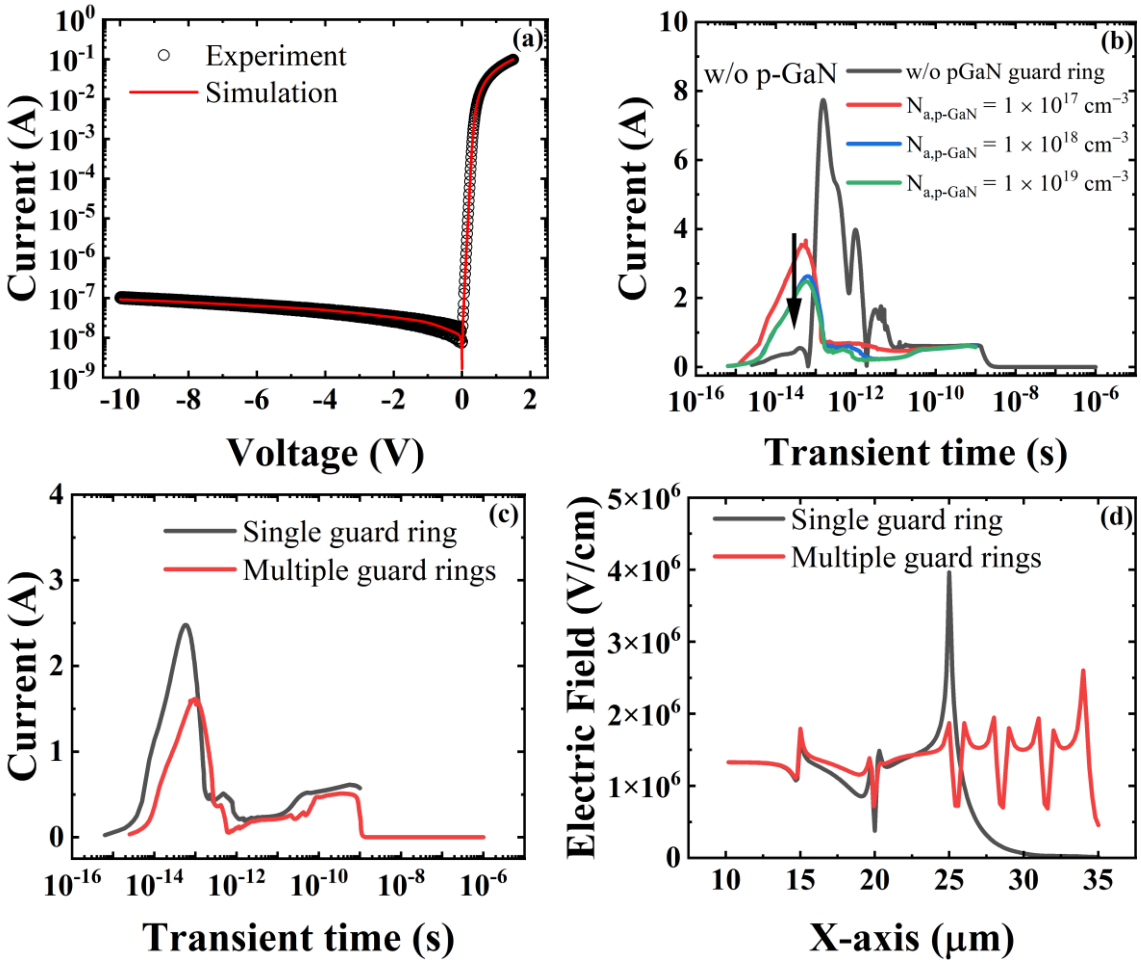

Figure 2 (a) Experimental and simulated I-V curves of GaN SBD w/o guard rings. TCAD simulations of (b) current vs. time for devices w/o and with p-GaN rings of different carrier concentrations. (c) Transient current and (d) electric field vs. distance for a single and multiple guard rings and p-GaN carrier concentration of 10^{19} cm^{-3}.

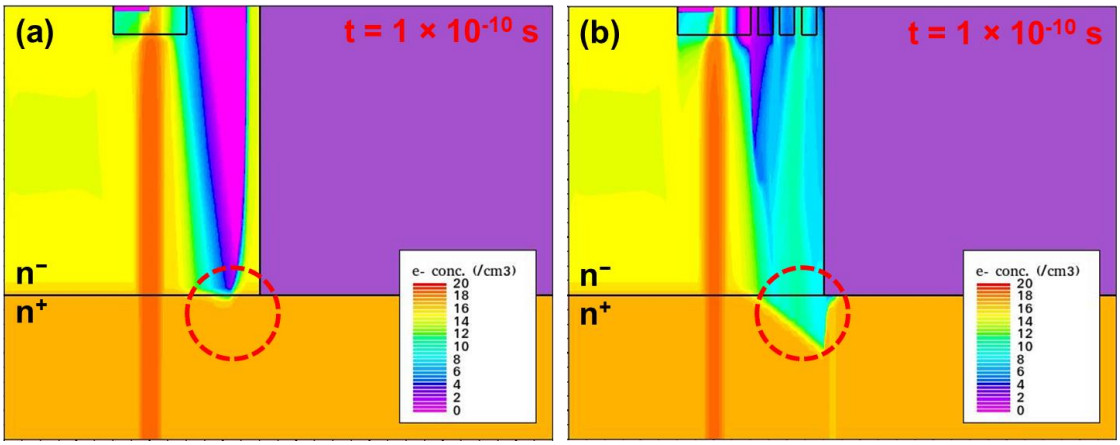

Fig. 3 The distribution of electron concentration for GaN SBDs with (a) single, (b) multiple guard rings.

Comprehensive study of electrons and spins bound to phosphorus donors in silicon-on-insulator nanostructures.

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The electronic and spin properties of phosphorus in silicon-on-insulator nanostructures are investigated.

Ultrathin silicon-on-insulator (SOI) layers play a relevant role in classical nanoelectronics [1], quantum computing [2], and, more recently, *in-materia* computing [3]. Properly engineering the key structural and material-related properties of the SOI, focusing not only on the doping level of the device layer but also on its thickness (varying here up to 50nm) and dielectric mismatch with the buried oxide or an additional top oxide layer, may lead to new phenomena, potentially innovating the design of nanoelectronic devices. In this work, we report on a systematic investigation of phosphorus-doped SOI nanostructures, combining theoretical calculations with experimental validation. The SOI structure is characterized by Si device layer, 155 nm SiO_2 buried oxide, and 525µm Si handle wafer. The device layer is P-doped by ion implantation, (energy 15 keV, fluence $1.4x10^{12}$ cm^{-2}), and subsequent furnace annealing at 1000°C for 5 min in dry nitrogen is performed. This results in a uniform doping level of the device layer ([P]=$3.4(9)x10^{17}cm^{-3}$), as verified by SIMS measurements. The I-V characteristics measured at different temperatures T are shown in Figure 1. An Arrhenius fit for 105K< T < 300K provides a donor activation energy of (45.8±0.5) meV, consistent with the value reported in literature for P-doped bulk Si [4]. This also indicates that the donors can be considered isolated [5]. The donor wave function is probed through the hyperfine interaction obtained from continuous wave electron spin resonance spectroscopy (CW-ESR). To improve the sensitivity, contact-less electrically detected magnetic resonance (CL-EDMR) was performed, and the resulting spectra are shown in Figure 2. Spin-dependent transport mechanisms will be also discussed, showing the result of EDMR measurements performed electrically contacting the sample. The theoretical study reproduces the SOI geometry, considering isolated P substitutional donors in a Si device layer confined by two insulator semi-infinite barriers of quantum well: $SiO_2/Si/SiO_2$. It is carried out within the effective mass approximation, where the ground state is calculated variationally with the donor electron's effective Bohr radius taken as the single variational parameter. Figure 3 (left) shows the calculated values of the effective Bohr radius and binding energy obtained variationally for device layer thicknesses varying from 50nm to 10nm. We find that narrower quantum wells lead to larger donor binding energies, keeping the delocalized nature of the shallow donor electron wave function. A first experimental confirmation comes from the CL-EDMR performed on an SOI with a device layer of (22.9±0.5) nm, obtained by wet etching, that shows no significant variation of hyperfine interaction with respect to the 50nm sample (Figure 3, right). An

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ongoing electrical characterization will verify the increase in activation energy predicted theoretically. Further investigations are also ongoing as far as the dielectric mismatch is concerned, both theoretically, considering different oxide barriers, and experimentally, by replacing the native top oxide, with different oxides grown by atomic layer deposition (ALD).

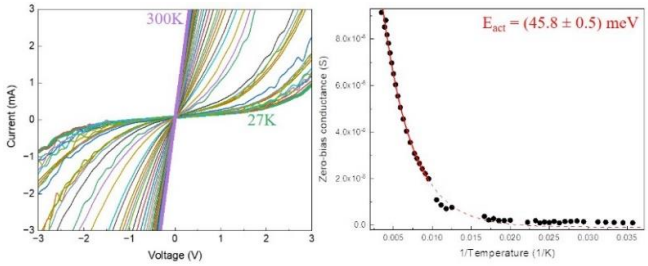

Figure 1: (Left) I-V characteristics as a function of the temperature. (Right) The fitting of the zero-bias conductance suggests a thermally activated charge transport mechanism.

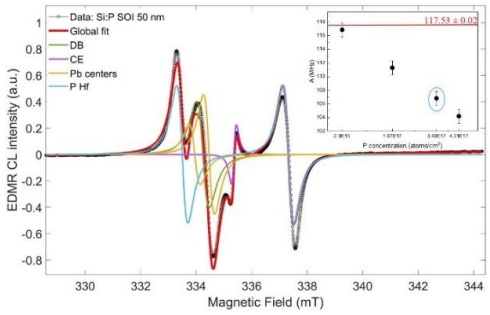

Figure 2: CL-EMDR spectrum of the SOI sample, measured at 4.2K. All the fitting components are indicated. The inset shows the reduction of the extracted hyperfine splitting for increasing donor concentration.

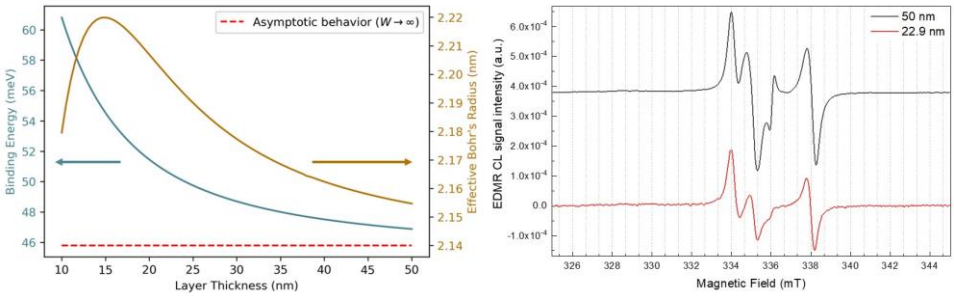

Figure 3: (Left) Calculated variational values of the activation energy and effective Bohr radius as a function of the device layer thickness, for a P donor located halfway between the quantum well interfaces. (Right) CL-EDMR spectra of the SOI samples with different device layer thicknesses, showing no significant variation of the hyperfine splitting.

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Maintenance-free energy source made of SOI wafers and piezoelectric materials: AlN:Sc and PZT

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Keywords: SOI-based devices, energy harvesting, piezoelectric materials, PZT, AlN:Sc

This paper presents our study on energy harvester devices made of silicon-on-insulator (SOI) wafers. The idea behind the harvester's design was based on a MEMS structure consisting of a thin silicon membrane-anchored on one side, with several piezocapacitors distributed on its surface.

Two approaches were applied: with a piezo layer made of lead-free material - aluminum nitride heavily doped with scandium (AlN:Sc) and lead zirconate titanate (PZT).
First approach (Fig. 1): the MEMS structures were fabricated on SOI wafers, which made it easy to control the membranes' thickness where the piezocapacitors were placed. The sputtered AlN:Sc As piezoelectric material was used in this case. The design of six independent capacitors allowed us to test several versions of their interconnections. Finally, the serial connection approach was found to be optimal. Placing all piezocapacitors on one membrane ensured each capacitor's in-phase conversion of vibrations into electric charges, maximizing the energy obtained. The MEMS membrane defined by the device layer thickness of 10 um had dimensions of 5x5 mm. The lower electrode was made of a 150 nm thick Pt layer. The AlN:Sc layer was ca. 1 um thick, and the top electrode was 300 nm thick Au. The proof mass was located at the "free end" of the membrane parallel to its edge and had a cross-section of 0.5x0.5 mm. Manufacturing of the structure was preceded by multi-domain simulations made in the CoventorWare 2010 program (Fig. 1a).

The obtained resonance structures exhibited a resonance frequency of approximately 300 Hz. Additional weights were mounted on the upper surface of the membrane to decrease the resonance frequency. Such a hybrid approach used a piece of ceramics with dimensions of 0.5 x 0.7 x 5 mm and a copper cylinder with a diameter of 1.3 mm and a length of 5 mm (Fig. 2b). The resonance frequencies of 157 Hz and 100 Hz were obtained, respectively. For the former frequency, a power density of 24 nW/mm2 was achieved with an acceleration of 2 g.

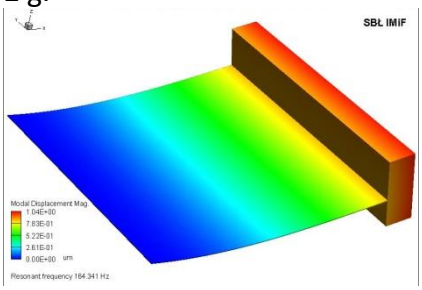
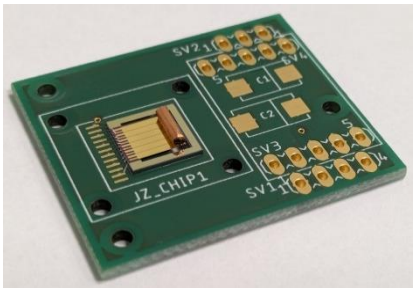
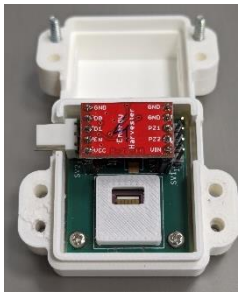


Fig. 1. a) Simulation results for resonant frequency;



b) The piezo-MEMS structure assembled on a dedicated PCB;



c) The piezoelectric harvester in dedicated package (open);

Second approach (Fig. 2): the MEMS structures were fabricated on SOI wafers as well. It allows us a superior control over the resulted resonant frequency. PZT-4D was used as piezoelectric material and it was obtained by PLD deposition. The resulted structure was a piezoelectric cantilever with a silicon proof mass at the “free end”. The thickness of the silicon substrate of the cantilever was 20µm. The energy from vibrations was harvested using a gold inter-digits electrodes (IDEs), deposited on the top of the piezoelectric layer. The IDEs have a thickness of 200nm and its widths and spaces between digits were chosen according to the thickness of the piezoelectric layer (~1.1µm of PZT-4D). These parameters were important in the polling of the piezoelectric layer. The silicon proof mass was obtained by etching in the same process with the overall structure. Its thickness was around 510µm, the thickness of the wafer, and its length was 70% of the length of the cantilever.

The obtained resonance structures exhibited a resonance frequency around 90Hz. In this case, the resonant frequency could not be easily tuned as in the first case. Its value is given by the silicon proof mass and it could be changed by redesigning a process mask. An additional ceramic proof mass could break the cantilever. The dimensions of the resonant structure were 8.8 x 7.45mm (Fig.2b). A power density of 30nW/mm^2 was obtained for a single structure, at an acceleration of 0.5g and a resonant frequency of 86Hz. Several structures could be connected in series or parallel.

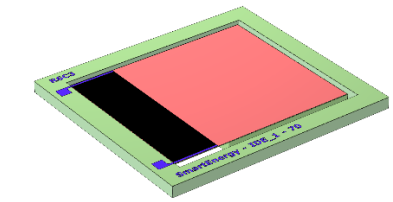
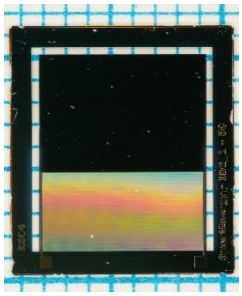
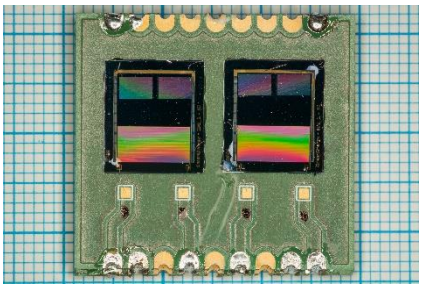


Fig.2. a) 3D model of the harvester;



b) Fabricated piezo-MEMS structure;



c) Structures mounted on a dedicated PCB;

The fabrication process flow for both energy harvester types based on SOI substrates, device performances, application and further assessment of the approaches taken will be discussed in detail.

Acknowledgements: The research work was supported by „SmartEnergy” M-ERA.NET.

Analog Behavior of V-FET operating in forward and reverse mode

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***Abstract*— This work investigates the analog parameters of p-type Vertical Field-Effect Nanowire Transistors (V-FETs) built on a Silicon-On-Insulator (SOI) wafer, focusing on variations in channel diameter (CD) and two different operational modes: forward (drain at top electrode) and reverse (drain at bottom electrode). When CD decreases from 40 to 20 nm in forward mode, the subthreshold swing (SS) improves from 93 to 76 mV/dec, the Drain-Induced Barrier Lowering (DIBL) also improves from 138 to 43 mV/V and the intrinsic voltage gain (A_V) increases from 19 to 34 dB. The reduction in CD enhances electrostatic control of the gate over the channel, leading to improved transistor characteristics. A significant impact of the access resistance at the top electrode is observed in forward mode. While forward mode presents an improvement in DIBL, V_{EA} and A_V, in the reverse mode shows better gm_{sat}, SS_{sat} and f_T. Additionally, the trade-off analysis between intrinsic voltage gain and unity gain frequency resulted in an optimal point at strong version for IC= 63, A_V=28 dB and f_T=2.6 GHz in forward mode, and for IC= 34, A_V=20 dB and f_T=3.7 GHz in reverse mode.**

Keywords- Vertical Nanowire, VFET, SOI, analog parameters.

I. INTRODUCTION

Aiming to explore new devices to advance technological scaling along with their good performance, vertical nanowire transistors (V-FETs) have proven to be quite distinctive and promising for this path [1]. This vertical configuration offers several advantages over traditional transistors, including reduced footprint, enhanced scalability, and potentially higher switching speeds. As a result, V-FETs have garnered significant attention in the semiconductor industry as a potential breakthrough technology capable of addressing the challenges posed by the relentless pursuit of smaller and more powerful electronic devices [2-3].

This work focuses on analyzing the analog parameters of V-FET devices by varying their configuration (forward and reverse mode), and by varying the channel diameter of the devices.

II. DEVICES CHARACTERISTICS

The V-FETs are p-type devices built on a silicon-on-insulator (SOI) wafer, with a buried oxide thickness of 145 nm, gate length (L_{gate}) of 50 nm and a channel diameter of 20, 30 and 40 nm [4]. The gate dielectric corresponds to an equivalent oxide thickness (EOT) of 0.9 nm. More information about the description of the process flow can be found in [5].

The V-FETs can be biased with two different configurations, one with the source as the bottom electrode (BE) – forward mode, as presented in Figure 1, and the other with the source as the top electrode (TE) – reverse mode.

III. RESULTS AND ANALYSIS

The V-FETs pMOS transfer curves were measured using B1500A from Keysight® with a gate bias (V_{GS}) from 0.5 V to -1.0 V, with a step of -10 mV and the drain voltage (V_{DS}) of -50 mV (triode region) and -700 mV (saturation region), at room temperature. The output characteristics were measured with a drain bias (V_{DS}) from 0 V to -1.0 V (-10 mV step) only for 200 mV of gate overdrive voltage ($V_{GT}=V_{GS} - V_T$, where V_T is the threshold voltage).

Figure 2 presents the transfer curves, I_{DS} x V_{GS} (A) and output characteristics, I_{DS} x V_{DS} (B). In forward mode there is a higher access resistance, which results in a smaller drain current, when compared to reverse mode, which is observed in both transfer curves. The drain current increases with channel diameter (CD) as expected, due to the increase in the perimeter.

Reducing the channel diameter improves the electrostatic coupling, which can result in a reduction in the threshold voltage (V_T) as presented in Figure 3 A. There is a reduction of 130 mV (reverse mode) and 140 mV (forward mode) from CD of 40 nm to 20 nm. When analyzing the DIBL (Drain-Induced Barrier Lowering) in Figure 3B, it is possible to observe that it reduces with CD reduction, due to better gate to channel electrostatic coupling.

The operation modes present a significant influence in DIBL, where in forward mode the DIBL is smaller (around 100 mV/V in average) than is reverse mode, since in forward mode there is a higher potential drop at the top electrode (drain) reducing the impact of the applied voltage (V_{DS}) at the drain/channel junction and threshold voltage, consequently reducing DIBL.

In reverse mode the subthreshold swing (SS) is slightly improved, as shown in Figure 4. In saturation (V_{DS}=700 mV) – dashed line, this influence is more significant achieving SS about 14 mV/dec lower in reverse mode than in forward mode.

Figure 4 also shows that the enhanced gate to channel control when reducing the channel diameter leads to an improvement in the SS, reducing its value from 93 mV/dec to 76 mV/dec (forward mode, V_{DS}=50 mV).

Figure 5 presents the normalized transconductance in saturation (gm_{sat}) as a function of subthreshold swing in saturation (SS_{sat}).

For a better performance is desired a high gm_{sat} and low SS_{sat}. Reducing the channel diameter improves the device performance by reducing SS and increasing normalized gm_{sat}. Due to the smaller access resistance associated at drain, the reverse mode presents an improvement in both parameters when compared to the forward mode.

In vertical nanowire transistors, the channel diameter plays a role in determining the electrostatic control of the channel and the overall transistor performance. Reducing the channel diameter, improves the electrostatic control, leading to better gate control over the channel [6]. This improved control can influence the Early voltage (V_{EA}) by affecting the rate at which the transistor enters the saturation region and the output conductance.

Figure 6 A presents the Early Voltage as function of channel diameter, where an improvement in V_{EA} is observed while reducing CD. Although the drain current is lower in forward mode, the Early voltage is higher, about 6.3 V, for CD=20 nm, while in reverse mode is about 2.1 V.

The intrinsic voltage gain (A_V) is defined by $|A_V|=gm/g_D \approx (gm/I_{DS})*V_{EA}$. Reducing CD, the electrostatic coupling is stronger, improving normalized gm. However, due to the direct dependence of gm with CD, the absolute value of gm decreases with CD. The better coupling also improves V_{EA} and the output conductance (g_D) which overcomes the gm one. As a consequence, A_V follows the V_{EA} tendency, presenting an improvement with CD reduction from 19 dB to 34 dB (forward mode). As A_V depends on V_{EA} it results in a higher intrinsic voltage gain in forward mode, of 34 dB, for CD=20 nm while in reverse mode it is 23 dB.

Once the channel diameter of 20 nm presented the better performance, it is presented in Figure 7 the trade-off between intrinsic voltage gain and unity gain frequency as a function of inversion coefficient IC.

This trade-off is particularly relevant in transistor-based amplifiers, where the transistor's internal capacitances and other parasitic elements affect the amplifier's bandwidth.

Figure 7 A, presents A_V as a function of IC, the maximum gain is obtained at weak inversion (IC<0.1), and decrease as IC increases.

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Once the unity gain frequency (f_T) depends on the transconductance ($f_T=gm_{sat}/(2\pi C_{gg})$,) it will be higher in reverse mode, as presented in Figure 7B, and its maximum value is at strong inversion.

When making the trade-off between A_V and f_T, it can be observed that the optimal point (maximum) takes place at strong inversion at around 30 IC for reverse mode and 60 IC for forward mode.

IV. CONCLUSIONS

This work highlights the crucial role of channel diameter and operational modes in shaping the performance of p-type V-FETs. The reduction in channel diameter enhances electrostatic control, resulting in improved transistor characteristics, as evidenced by reduced subthreshold swing (SS) and enhanced intrinsic voltage gain (A_V).

The forward mode presented a higher access resistance when compared to reverso mode, causing a degradation in SS and transistor efficiency, in contrast, the forward mode was improved for DIBL, V_{EA} and A_V.

The trade-off analysis between A_V and f_T presents an optimal performance achieved at strong inversion. These results contribute valuable insights into the design considerations for transistor-based amplifiers, where the trade-off between intrinsic voltage gain and unity gain frequency is crucial for optimizing overall performance.

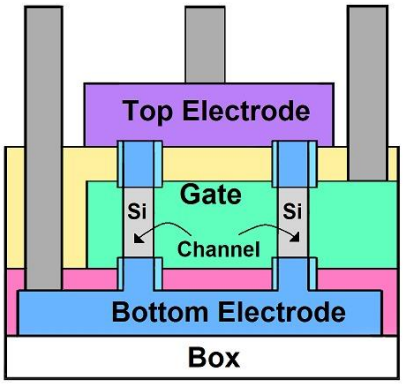

Figure 1 - schematic cross section of V-FET.

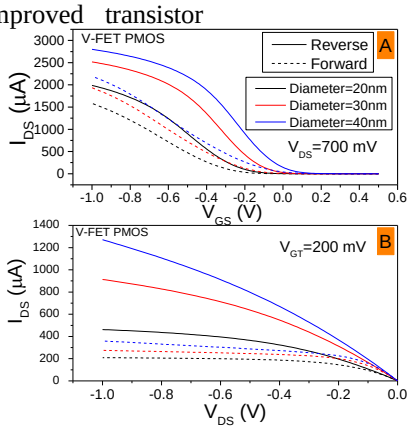

Figure 2 – Drain current as a function of gate voltage (A) and drain voltage (B), in forward and reverse mode for channel diameter of 20, 30 and 40 nm.

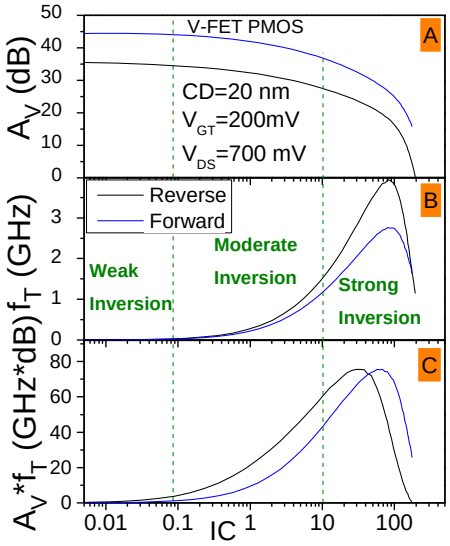

Figure 7 - Intrinsic voltage gain (A). unity gain frequency (B), trade-off between intrinsic voltage gain and unity gain frequency (C) as a function of inversion coefficient, in forward and reverse mode, for channel diameter of 20 nm.

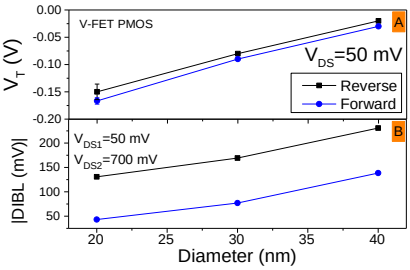

Figure 3 – Threshold voltage (A) and Drain-Induced-Barrier-Lowering as a function of channel diameter, in forward and reverse mode.

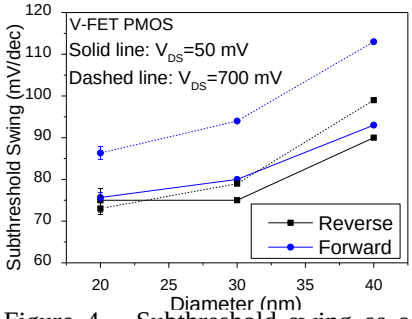

Figure 4 – Subthreshold swing as a function of channel diameter in forward and reverse mode, for drain voltages of 50 mV and 700 mV.

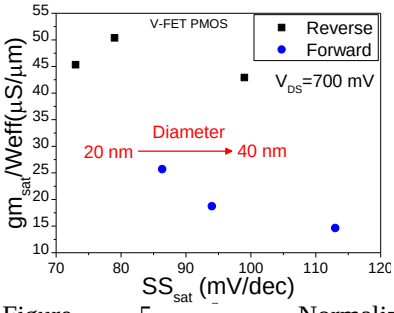

Figure 5 – Normalized transconductance (V_{GT}=200mV) as a function of subthreshold swing, for channel diameter of 20 nm, 30 nm and 40 nm, at V_{DS}=700 mV, in forward and reverse mode.

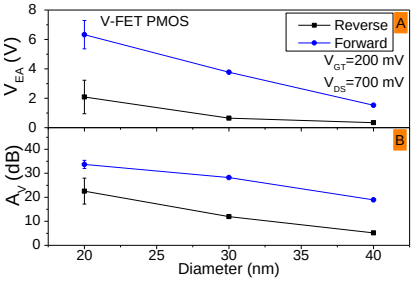

Figure 6 – Early voltage (A) and intrinsic voltage gain (B) as a function of channel diameter, in forward and reverse mode.

ACKNOWLEDGMENT

The Brazilian authors acknowledge CNPq, CAPES and FAPESP (2020/04867-2) for the financial support. We also thanks imec CMOS technology program members and the amsimec test labs for their support.

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An Ultra-Low Power VCO for RF Sensing Application

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VCOs play an indispensable role in modern-day RF and microwave applications. Specifically, VCO employed for bio-Medical applications must exhibit high spectral purity while consuming lower power to optimize battery performance [1]. This abstract describes an experimental Ultra-Low power VCO implemented in 22-nm CMOS FDSOI technology, operating from 10 GHz to 14 GHz for a tuning voltage ranging from 0.1 V to 1.2V. The current VCO tuning response can be modified with an additional frequency multiplier or a frequency divider to target a wide range of applications (Figure 1).

The adoption of lower-node 22-nm CMOS-FDSOI technology has significantly enhanced the feasibility of ultra-low power RFICs with diverse applications in the field of bio-medical sensing. Furthermore, this approach enables seamless integration of RF blocks with other mixed-signal functionalities [2].

The current VCO employs a cross-coupled topology with a resonator comprising of two differential Inductors: L1 (Top-Inductor), L2 (Tail- Inductor), along with NCAP-SOI varactors. The primary coil L1 (Figure 3: blue) is based on a single thick copper metal ensuring less resistance from the vias and offering stable Inductance and Quality factor (QF) for the required operating frequency range. The tail inductor L2 (Figure 3: red) is a custom differential inductor with two stacked copper layers, serving two main purposes: rejection of the fundamental's second harmonic present at the common node; provides a secondary tuning voltage (V_{tune2}) for fine tuning of frequency and enhancing the noise behavior. Additionally, two reverse-bias diodes are employed to prevent back-feeding of power supplies under fault conditions. The output of the VCO is cascaded with a similar cascode buffer in [3] to enhance output power and isolate the VCO core from random output load variations.

Preliminary measurement results of the VCO indicate that it is functional from 9.3 GHz to 12.8 GHz, for a tuning voltage range from 0 to 1.1 V (Figure 5 and Figure 6) and an applied supply voltage of 750 mV. The simulated average output power is -12.7 dBm. At the frequency of 10 GHz the lowest phase noise of -98.9 dBc/Hz @ 1 MHz offset is simulated (Figure 4).

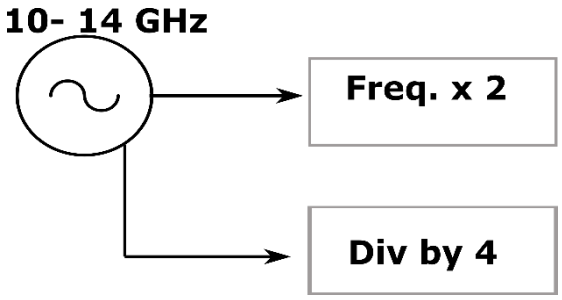

Figure 1: Prospects for the proposed VCO.

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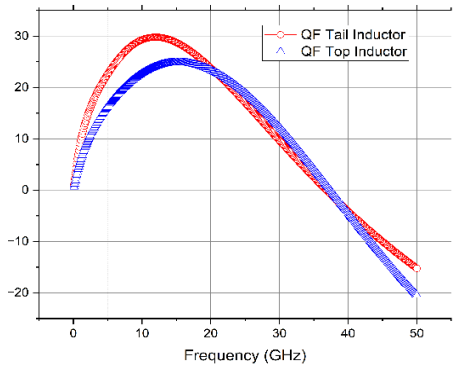

Figure 3: Quality factor of L1 (blue) and L2 inductors (red).

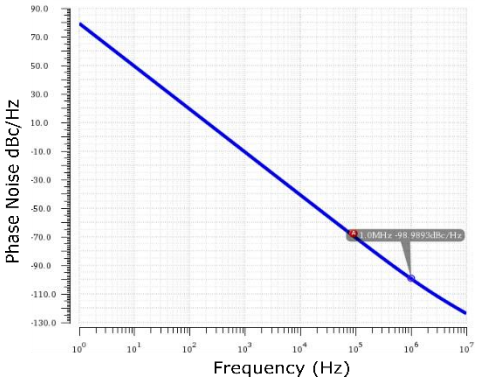

Figure 4: Simulated phase noise response @1 MHz offset for the current VCO.

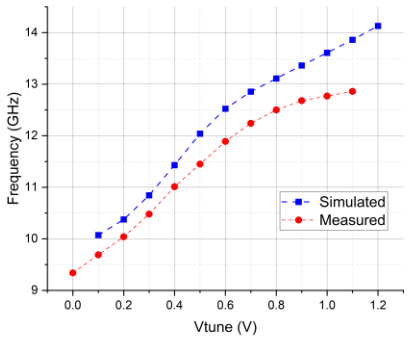

Figure 5: Simulated and Measured Frequency Variation with Tuning Voltage (Vtune1).

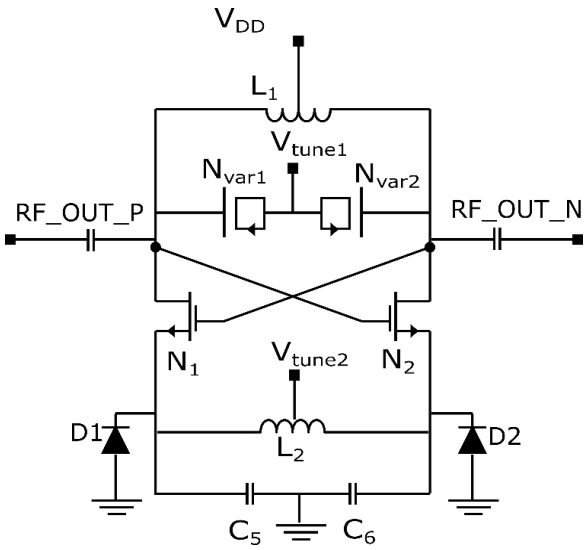

Figure 2: VCO Schematic.

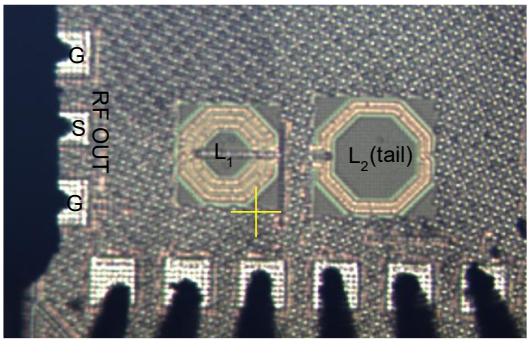

Figure 6: Die Photo of the DUT (VCO).

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Impact of Source-Drain Series Resistance on Carrier Mobility in AlGaN/GaN High Electron Mobility Transistors

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Abstract

This work presents an analysis of the impact of source-drain series resistance (R_{SD}) on carrier mobility (μ_n) in AlGaN/GaN High Electron Mobility Transistors (HEMTs). The study also shows the influence of channel width (W) and channel length (L_g) on the R_{SD} of the device. In the research it was observed that the R_{SD} is greater in devices with higher L_g and lower W and that its increase causes a reduction in μ_n, which consequently decreases the efficiency of the device.

1. Introduction

The series resistance (R_{SD}) has an influence on the μ_n. The relationship between R_{SD} and μ_n can be observed according to equation 1, where S is the subthreshold slope, V_d is the drain voltage and C_d is the depletion capacitance [1].

$$\mu_n = S(1 - R_{SD} V_d S)^{-1} (C_d W/L_g)^{-1} \quad (1)$$

2. Device description and experimental results

The AlGaN/GaN HEMT under study is described in Fig. 1 [2]. Fig. 2 shows that I_d is higher in HEMTs with lower L_g and higher W and as seen in Fig. 3, the output conductance (g_d) will have the same behavior, which means that the device geometry has a great influence on current amplification. In Fig. 4 it is observed that the higher the R_{SD}, the lower the μ_n, because when the R_{SD} is high, it reduces the effective gate voltage, making carriers movement difficult. $R_{SD}$was obtained through algebraic calculation, isolating it from equation 1, and the other parameters were extracted through the $I_d x V_g$ and $I_d x V_d$ curves of the devices measured in imec (Interuniversity Microelectronics Centre).

3. Conclusions

The greater the R_{SD}, the greater the limitation on the maximum current that can flow through the circuit causing a decrease in μ_n. Therefore, minimizing R_{SD} is essential to optimize transistor performance, which can be done by optimizing the channel geometry.

Acknowledgments

Thanks to imec for providing the samples. Also, thanks to CAADI (Coordination of Affirmative Actions, Diversity and Equity), the Brazilian research-funding agency CAPES and FAPESP (Process Nº: 2023/00123-7).

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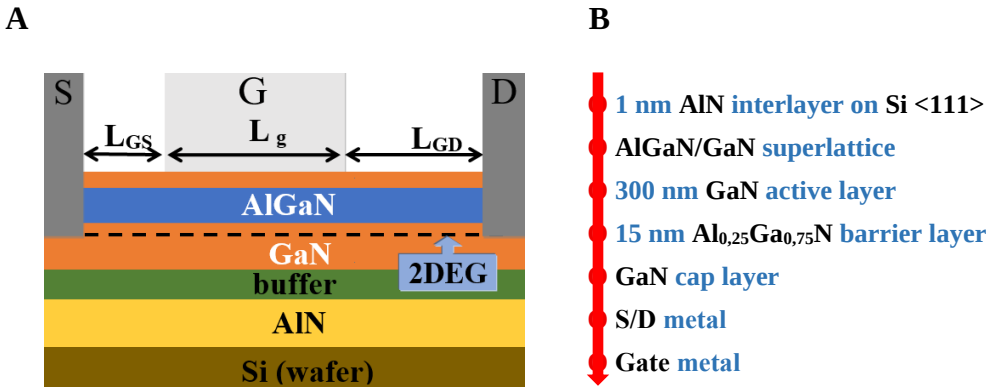

Fig. 1. (A) HEMT device structure and electrode materials. Schematic diagram (B) of the fabrication process flow of the HEMT devices [2].

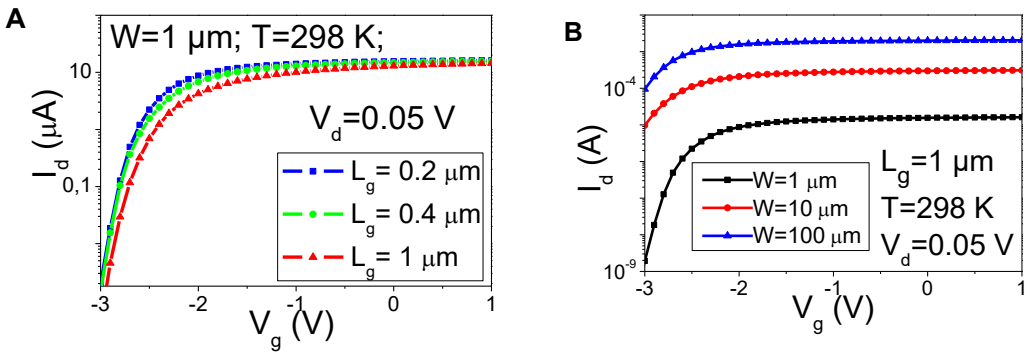

Fig. 2.Current versus gate voltage ($I_d x V_g$) with variation of (A)-L_g and (B)-W.

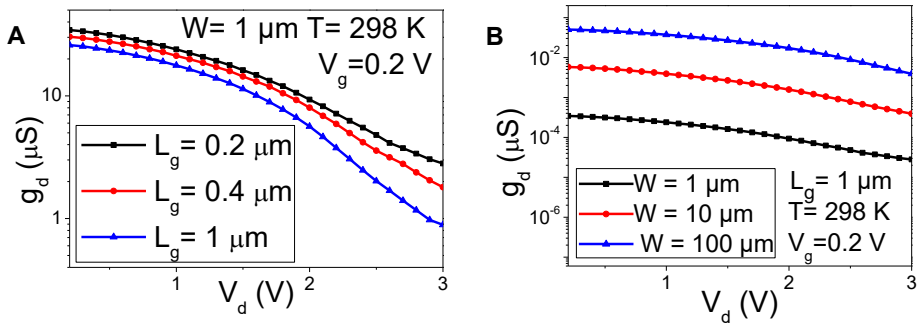

Fig. 3. Output conductance versus drain voltage ($g_d x V_d$) with variation of (A)-L_g and (B)-W.

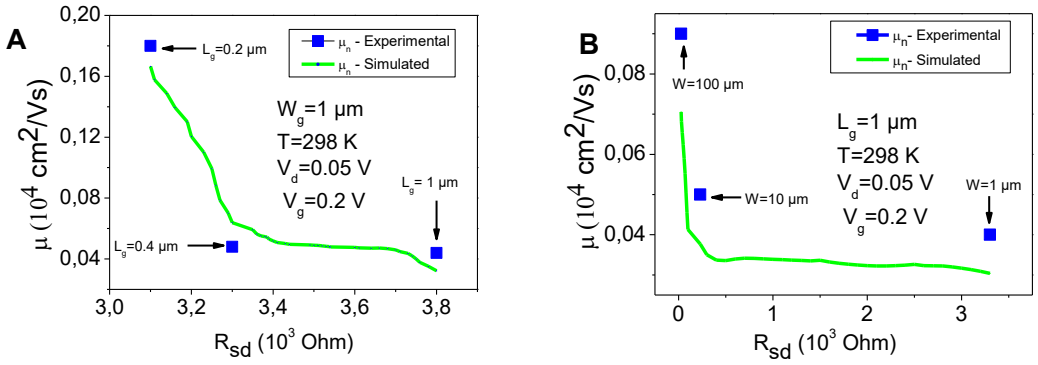

Fig. 4. Experimental and simulated values of $\mu_n x R_{SD}$ with variation of (A)-Lg and (B)-W.

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Coupling ab-initio Description and Monte Carlo Simulation to Capture the Transport of Hot Carriers

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Efficiency of standard solar cells is limited by their inability to exploit all the excess energy of photo-induced carriers, and that can be solved by considering hot carrier solar cells instead [1]. In this context, a new methodology that can accurately study the evolution of hot carriers in a wide range of semiconductors is needed. A Full Band Monte Carlo (FBMC) simulator [2], which originally uses band structure and electron-phonon scattering rates calculated by Empirical Pseudo Potential Methods (EPM) and analyzes only the stationary regime, is now improved to read calculations from Density Functional Theory (DFT) and study also transient regimes. In this preliminary work, the introductions of the DFT band structure and a sampled scattering matrix that considers the coupling of all initial k and final k'-states are tested.

A DFT-based electronic band structure derived from Quantum Espresso, using a 16x16x16 k-point grid and local density approximation (LDA) for a GaAs lattice constant of 5.53Å, is implemented in the MC code. Figure 1, shows a similar evolution for the first conduction band between EPM and DFT, leading to similar effective masses of 0.06m0 (EPM) and 0.05m0 (DFT).

Secondly, to implement DFT scattering rates in the MC code, it is first mandatory to be able to handle the full scattering matrix S(k,k'). To test our methodology, the S(k,k') matrix is first calculated using EPM according to a given band structure. In addition, a rejection technique that was commonly used to save computation memory is compared with more rigorous approach that takes into account the exact probability of the final state, i.e. using the distribution given by S(k,k'). The FBMC algorithm is shown in Fig. 2.

Next, the velocity versus field curve using different band structures and techniques is analyzed (Fig.3). At low fields, where effective mass has a significant impact on velocity, all results remain close to experimental findings [3]. At high fields, different band structure gives different intervalley scatterings, which explains the greater discrepancies between the results. However, the DFT band structure gives closer results to the experimental findings. Moreover, the technique used plays a crucial role at this range of field and the relevance of using the rejection technique is questionable. Fig.4 illustrates carrier energy relaxation over time. Substituting all inputs with DFT data is expected to produce results that match experimental outcome [4] for the energy loss rate of hot carriers.

To conclude, we are developing an FBMC code for the analysis of hot carriers in transient regimes, ready to exploit ab initio calculations. The DFT band structure and the full band scattering matrix S(k,k') have been introduced. In the next steps, ab-initio DFPT electron-phonon scattering rates will replace the empirical scattering rates. Once GaAs has been properly described, this code will be extended to the study of transient regimes in 2D materials.

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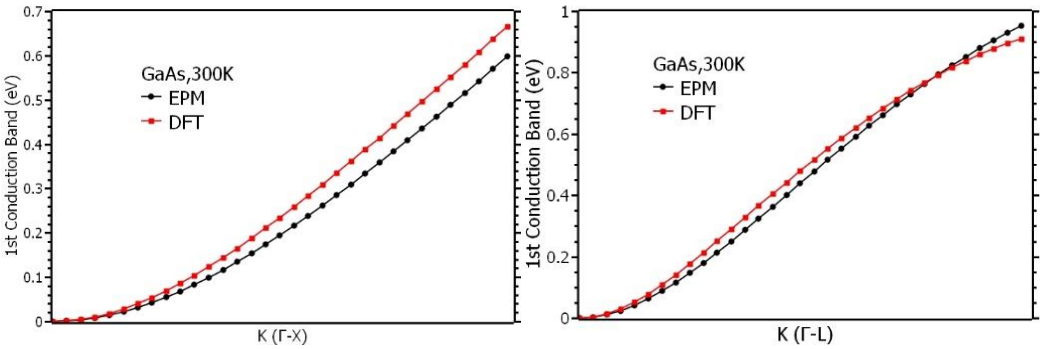
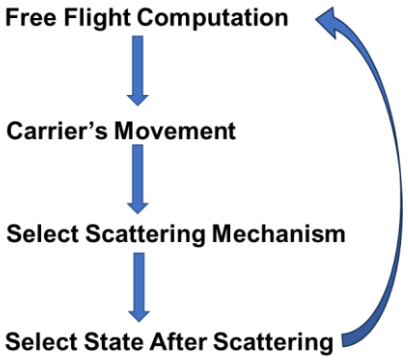


FIGURE. 1. Energy values of the first conduction band with respect to states along (a) Γ-X and (b) Γ-L directions calculated with EPM and DFT.

(a)



(b)

$$S_i(\vec{k},\vec{k'}) = \frac{2\Pi}{\hbar}\left|\langle\vec{k'}|H_i|\vec{k}\rangle\right|^2 \varphi_{k'}\,\delta(E' - E - \hbar w i)$$

Where:

$\vec{k}$, E are the initial state and energy respectively.

$\vec{k'}$, E' is the final state and energy respectively.

H_i is the electron-phonon interaction Hamiltonian.

$\varphi_{k'}$ is the final state density.

$\hbar w$ is the phonon energy.

FIGURE. 2. (a) Sketch of the Monte Carlo code algorithm. (b) Fermi Golden rule scattering rate from initial state k to final state k'.

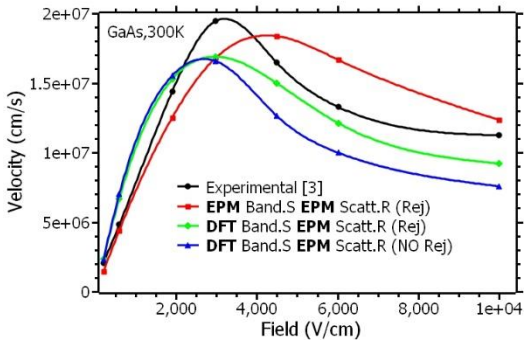


FIGURE. 3. Velocity versus electric field at stationary regime for different band structures and techniques.

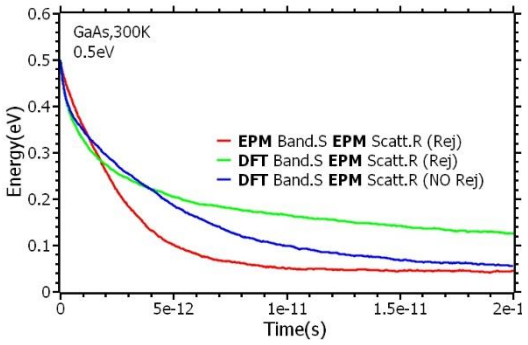


FIGURE. 4 Energy relaxation of carriers (initial energy 0.5eV) with time for different band structures and techniques

Recent developments on Thermoelectric devices based on Silicon

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For the Internet of Things (IoT) revolution to be fully deployable, one of the major challenges is the sustainability and the long-term autonomy of its power supply. In this context, thermoelectric harvesting is an alternative to primary batteries for powering sensor nodes with energy requirements in the sub-Watt range.

In this contribution, we present the work developed on the fabrication of thermoelectric structures based on Si nanowires (NWs), Si beams and nanostructured ultra-thin Si films.

Earlier, the group developed all-Si based micro-thermoelectric generators (µTEGs) with planar architecture starting from SOI wafers [1]. These, unlike standard vertical TEGs, engineer the heat flow to have a lateral temperature gradient that is harvested by an array of Si nanowires (NWs) or beams. This approach benefits from Si technologies for the downsizing and scalability, and from the fact that Si is abundant and environmentally sound. In order to fabricate a µTEG that fulfills the power needs of the IoT at the microscale (10-100 µW/cm^2), in this work we have integrated four µTEGs with Si beams in a single device (Fig.1). The use of custom Si adapters enables the integration of a bigger heat sink, which enhances greatly the power output of the µTEG, that produces now > 2 µW when exposed to T < 150 ºC.

Nonetheless, these Si beams and NWs are far from the best thermoelectric Si structure: rough surface Si NWs. However, this structure remains unused in TEGs due to its low-volume and non-reproducible fabrication. Patterning ultra-thin Si films by means of block copolymer (BCP) nanostructuration, instead, emerges as an attractive alternative, as it excels in scalability and reproducibility [2] and could match the overall thermoelectric enhancement of rough NWs [3]. To fabricate the Si membranes, we start from a SOI wafer with an ultrathin device layer (17 – 50 nm). A 30 nm block copolymer (BCP) film based on polystyrene-block-polymethylmethacrylate (PS-b-PMMA) is self-assembled perpendicularly oriented to the Si surface with cylindrical or lamellar morphology and a period between 28 and 80 nm. After, the PMMA is selectively removed and the PS is used as a mask in a reactive ion etching that transfers the pattern onto the Si layer beneath (Fig.2). Finally, the Si films are suspended with a KOH etching. To dope the films, we have explored the spin-on-dopant procedure, a cost-effective, sustainable and non-destructive process.

The doping values obtained with the spin-on-dopant method are in the optimal range for thermoelectric applications, 10^{19} – 10^{20} cm^{-3}, and can be adjusted with the temperature during the dopant's diffusion step. We have studied the electrical resistivity increase, consequence of the nanostructuration, and obtained values between no increase and a factor of 2, depending on the period and depth of the used patterns. Their thermal conductivity will be evaluated using the 3ω Völklein approach (Fig.2c) to study the effect of surface nanostructuration on thermoelectric performance.

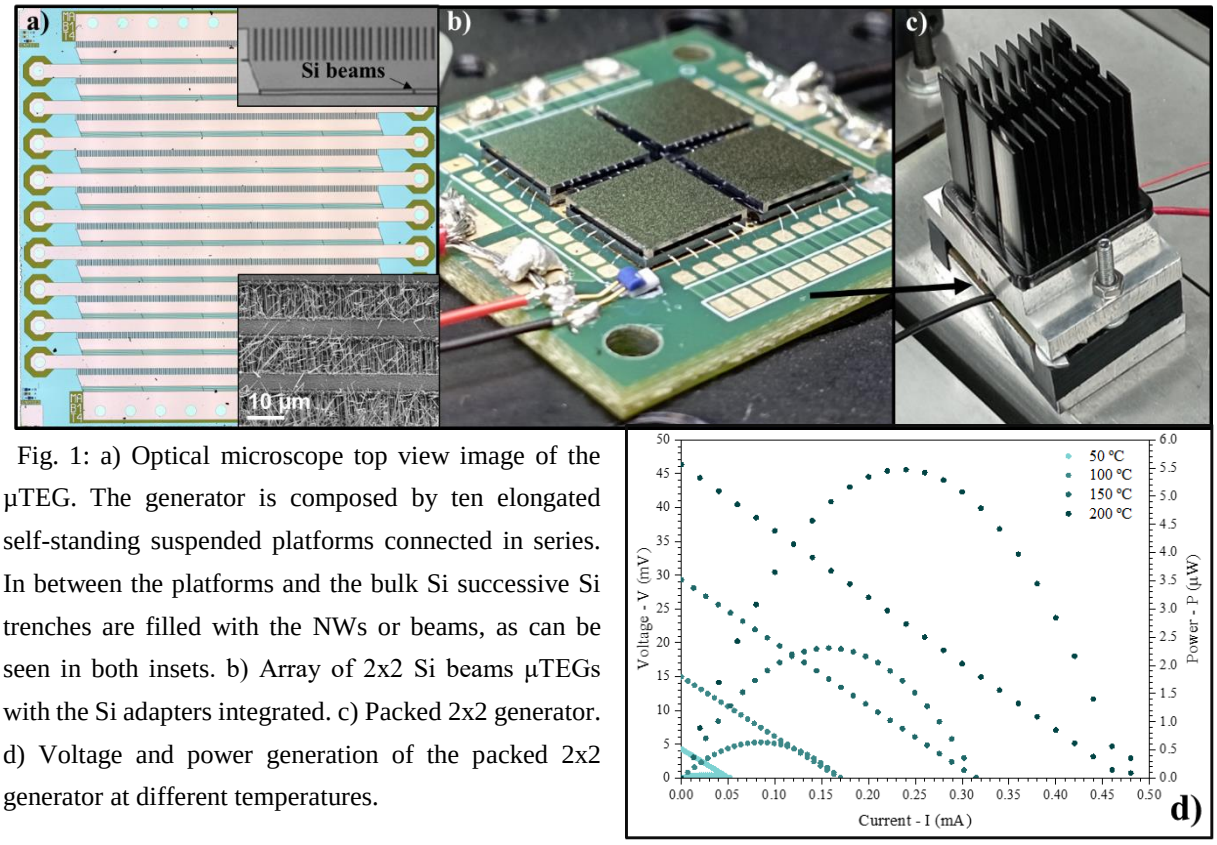

Fig. 1: a) Optical microscope top view image of the µTEG. The generator is composed by ten elongated self-standing suspended platforms connected in series. In between the platforms and the bulk Si successive Si trenches are filled with the NWs or beams, as can be seen in both insets. b) Array of 2x2 Si beams µTEGs with the Si adapters integrated. c) Packed 2x2 generator. d) Voltage and power generation of the packed 2x2 generator at different temperatures.

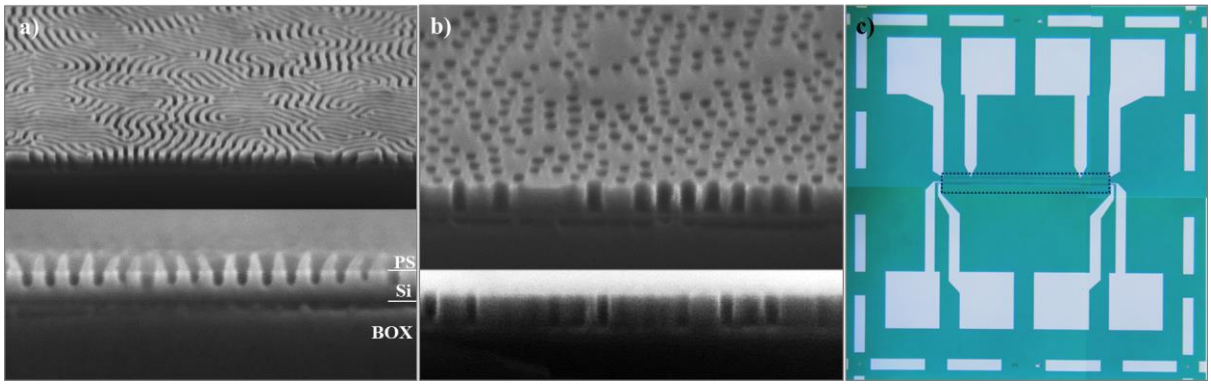

Fig. 2: a) SEM images of a 50 nm Si film etched following the fingerprint-like pattern of the PS mask. The etching of 25 nm, lower than the 50 nm thickness of the film, is done to diminish the thermal conductivity of the sample while at the same time maintaining electrical conductivity in between both sides of the film, enhancing its TE properties. b) SEM images of a 50 nm Si film etched following the cylindrical pattern. In this case, complete etching is done, since, due to the hole's distribution in the matrix, electrical conductivity is maintained through the film. c) Optical image of the chip fabricated to do the 3w characterization. The dotted line indicates the suspended membrane, where heater and sensor metallic stripes measure the ΔT on the nanostructured film.

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Monte Carlo Simulation of Thermoelectric Properties of Nanostructures

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Thermoelectric (TE) conversion has emerged as a promising phenomenon, particularly for low voltage devices. The efficiency of these TE devices is assessed using the figure of merit $ZT = S^2\sigma T/k$, where S, σ, T, and k represent the Seebeck coefficient (thermopower), electrical conductivity, temperature, and thermal conductivity of the device, respectively. While bulk silicon has long been studied as a TE material, its ZT value of 0.01 [1] falls short for practical applications. Numerous factors influence this efficiency, such as the device's size, doping level, and temperature gradient.

For having the ability to study the influence of the different mentioned factors on the TE properties, we use a self-consistent electron-phonon transport model. An ensemble Monte Carlo solver for electrons is coupled with a phonon baths that can have a non-uniform temperature. In this simulator presented in [2], electron-phonon scattering rates depend on the local temperature and the boundary conditions are also temperature dependent. Using this simulation tool, the TE properties can be studied, at the microscopic level, in doped silicon nanostructures of different size and with different types of interfaces.

In Fig. 1, a silicon nanofilm of doping 10^{18} cm^{-3} having a length of 100nm in the cross plane configuration is schematized. The device is sandwiched between 2 ohmic contacts at both ends that are also silicon but with doping of $10^{20}cm^{-3}$ which will serve as a reference for the extraction of the Seebeck coefficient. Thermal gradient (290K-310K) and voltage differences are applied between contacts. In Fig. 2, the corresponding IV curve is shown. A mobility and Seebeck coefficient of 223 $cm^2/V.s$ and 319 μV/K respectively were extracted that are comparable to those of [3].

The interest of the presented particle MC approach is that it can provide a deep insight of the TE transport at the microscopic level. For instance, electron density, kinetic energy, average velocity, and electrostatic potential along the device are plotted in Fig. 3 and 4. The relative contribution of the non-uniform temperature profile and voltage bias can be observed on the kinetic energy evolution. The kinetic energy increases with an increase of voltage.

The impact of size, doping, and temperature on the Seebeck coefficient will be investigated using this original tool and presented. In future work, phonon drag effects will also be implemented in our simulator which will give more accurate tool to optimize TE device performance in nanostructures.

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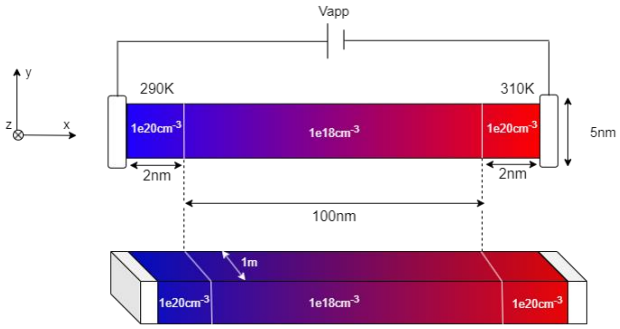

FIGURE. 1. (a) Schematic view of the TE device studied

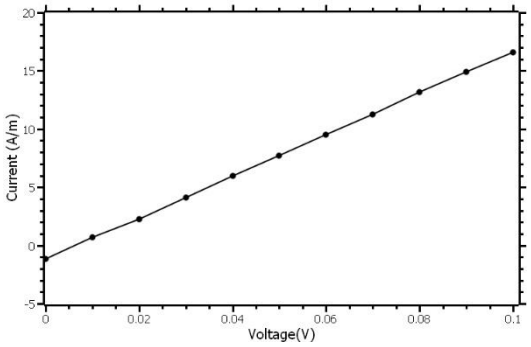

FIGURE. 2. Current obtained with respect to applied voltage for the studied device

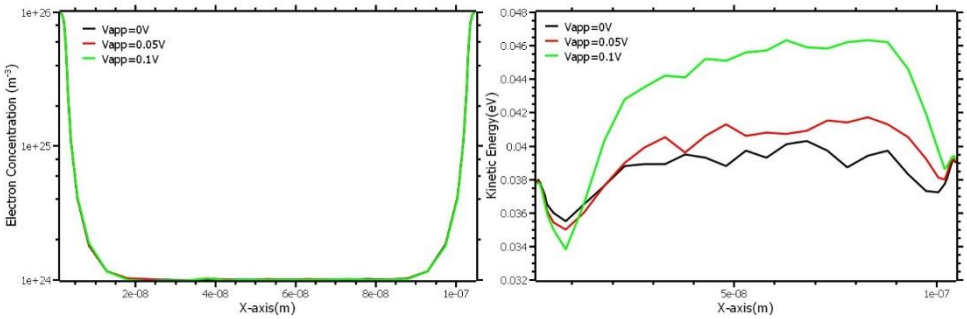

FIGURE. 3. Electrons (a) concentration and (b) kinetic energy versus device's length.

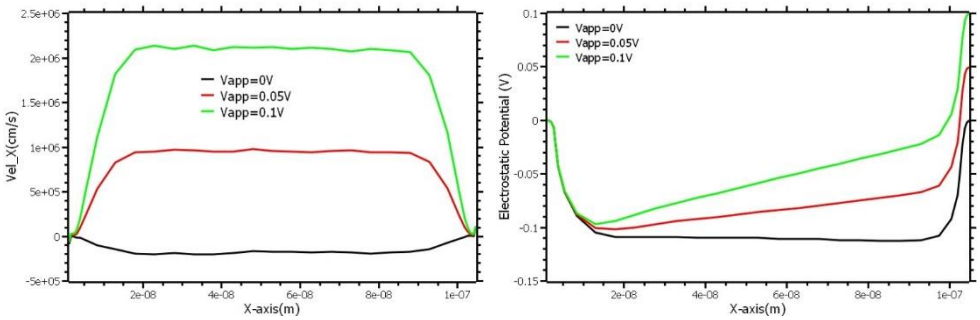

FIGURE. 4. Electrons (a) velocity along the direction of transport and (b) potential created versus device's length.

Stress management in freestanding membranes obtained by ion implantation induced delamination

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The Smart-cut™ technology has now become the main process used in microelectronics to obtain SOI substrates. This process involves the transfer of a thin film from an implanted donor substrate to a receiver substrate. The bonding step between the two substrates ensures that the thin film to be transferred is always held by a substrate. The same kind of implantation process [1] can be used to obtain freestanding thin films required from some applications such as MEMS, flexible electronics, 3D integration etc [2][3]. However, specific problematics arise when the thin film is no longer held by a substrate. Indeed, ion implantation induces in-plane compression stress in the "donor" substrate in the region of maximum gas concentration. Part of this stress remains after crack propagation and detachment of the film from the substrate. We show in this paper that a thin freestanding membrane is very sensitive to this stresse and it is therefore necessary to manage it.

We produced centimeter-scale freestanding thin films (1 µm thick) using ion implantation induced delamination, based on specific implantation conditions [1]. When the film is detached from its donor substrate, the stresses added by the gas implantations become directly visible, producing a rolling of these membranes on themselves (**Fig.1**). In contrast to standard substrate transfer cases, where two-dimensional stresses result in a small spherical bow of the substrate, the stress of the freestanding membranes is directly seen as a strong one-dimensional curvature. Indeed, for a SOI-type assembly, stress moment is applied to the whole thickness of the substrate while for freestanding membranes stress is balanced only by the thickness of the thin film. The dependency of curvature (1/R) on stress moment (σ t) is directly expressed by the Stoney formula [4] in function of E (Young Modulus), h (thickness of the study substrate) and ν (Poisson's ratio) :

$$\sigma t = \frac{Eh^2}{6(1-\nu)R} \text{ (biaxial stress) \& } \sigma t = \frac{Eh^2}{6R} \text{ (uniaxial stress)}$$

In our freestanding case, thickness h is 3 order of magnitude smaller than for wafer transfer, which ends up in millimetric radius of curvature which can be directly measured on the sample. In this case, bending is cylindrical and we use uniaxial Stoney's formula. Assuming the stress is distributed over a thickness t of 100nm, this corresponds to stress value close to 300MPa after the thin film delamination (i.e point at 500°C on the figure 2).

To release this stress, we annealed the samples at higher temperatures in order to cure implantation related defects and allow the implanted species to diffuse out of the thin film. **Fig.2** shows the evolution of curvature as a function of the annealing temperature applied. Above 700°C, all samples are essentially flat and stresses are relaxed from our freestanding thin film. This thin film can then be manipulated and for example bonded to a foreign substrate as shown on **Fig.3**. This type of process makes it possible to decouple the bonding and transfer steps (mandatory in the Smart-Cut™ technology),

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and e.g. transfer silicon thin freestanding films onto other types of material (soft substrates, plastics, heterostructures etc.).

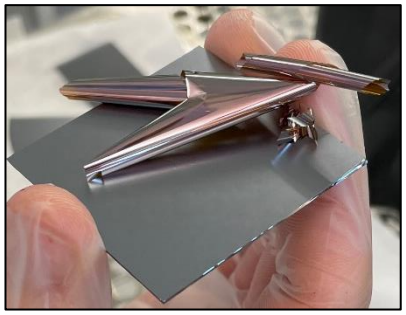

Fig. 1: (left) Image of a 5x5cm² silicon thin film rolled because of the uniaxial post-implantation stress

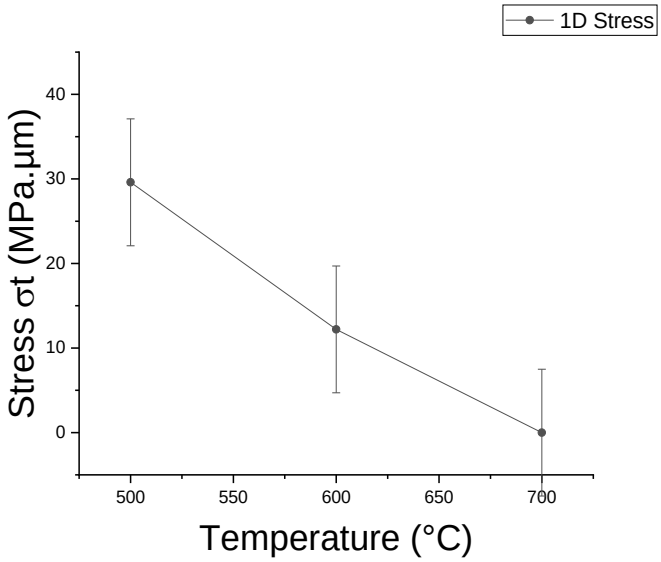

Fig. 2: Temperature evolution of the σ×t product as extracted from the 1-d curvature radius of delaminated membranes (solid circles)

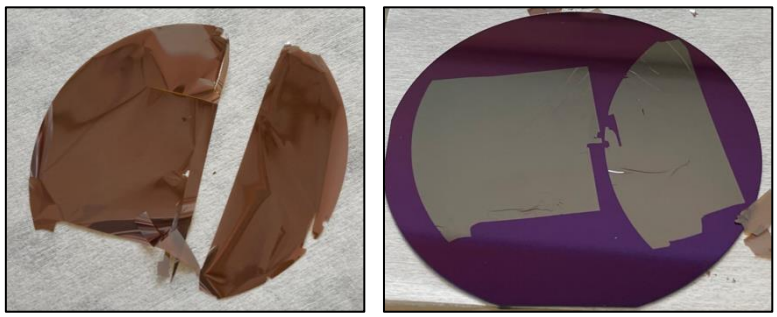

Fig. 3: (left) Cracked circular 100mm freestanding silicon thin film relaxed from stress after thermal anneal; (right) Picture of this previous freestanding thin film transferred onto a 100mm substrate

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Low power CO_2 detection for sensor integration on FDSOI-CMOS technology for of real-time air quality monitoring

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Nowadays, the levels of atmospheric air pollution have reached unprecedented thresholds. Emissions, notably CO_x and NO_x, originating from vehicles, industrial activities, and combustion processes, are primary contributors to this trend. These pollutants pose significant health hazards, including respiratory ailments, cardiovascular complications, and premature mortality. Consequently, there's an urgent imperative for robust air quality monitoring systems. Addressing this need, the gas sensor market endeavors to produce cost-effective, energy-efficient sensors capable of reliably detecting pollutants. Such advancements are indispensable for safeguarding public health and combating the adverse effects of air pollution.

In the light of the escalating demand for rea-time measurements and the rise of Internet of things (IoT) technology, the use of ultra-sensitive and ultra-low-power sensors offers tangible advantages. Current gas sensors, however, typically operate under high temperatures, such is the case of MOX sensors which generally require heating beyond 250°C, as imposed by their sensing layer activation energy. The search for a newer material with a lower operating temperature has been the goal of various research works. In this aspect, there are promising polymer-based hybrid materials like polyethylenimine-silica (Fig.1) can be utilized to circumvent the need for high temperatures in the detection of carbon dioxide [1]. When tested in an interdigitated electrode capacitive sensor, this material showed strong response (52%) to 2000 ppm concentrations of CO_2, as described in (Fig.2), with a relatively low response and recovery times (45s and 55s respectively) all while operating at temperatures down to 30°C.

This work focuses on the optimization of the sensing materials and their integration in a Gas-FET sensor using Fully Depleted Silicon on Insulator (FD-SOI) transistors [2] procured by STMicroelectronics. The strong capacitive coupling between the front and back-gate in these device enables the amplification of the potential present on the sensing gate by a factor of about 13 (Fig.3), thus unlocking the potential for highly sensitive sensors.

A cleanroom CMOS-compatible process has been developed for the back-end-of-line (BEOL) fabrication (Fig.4), with electrical characterizations, and eventually gas characterizations in a controlled environment using dedicated equipment.

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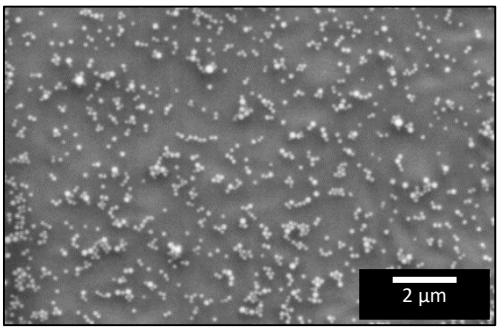

Fig.1: SEM image of the CO_2 sensitive Polyethylenimine-SiO_2 nanoparticles hybrid material showing a uniform distribution of the 150 nm silica nanoparticles in the polymer.

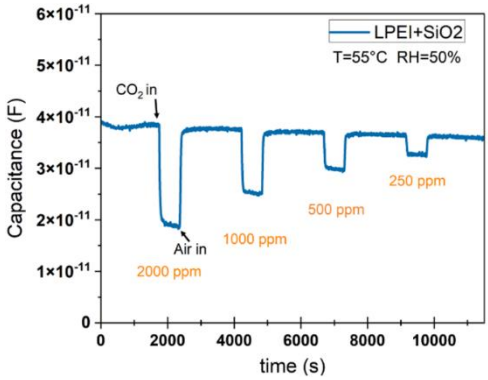

Fig.2: CO_2 Dynamic response of the PEI-SiO2 sensing layer mounted on an IDE sensor

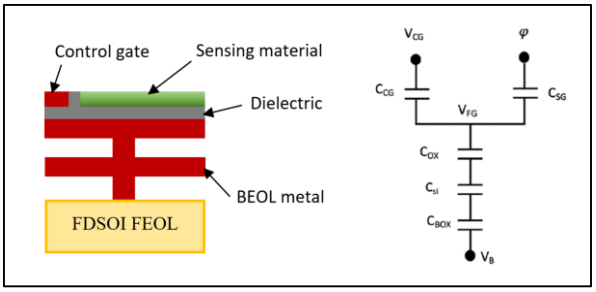

Fig.3: schematic diagram of the capacitively coupled sensor structure (left) with the capacitive divider equivalent circuit (right)

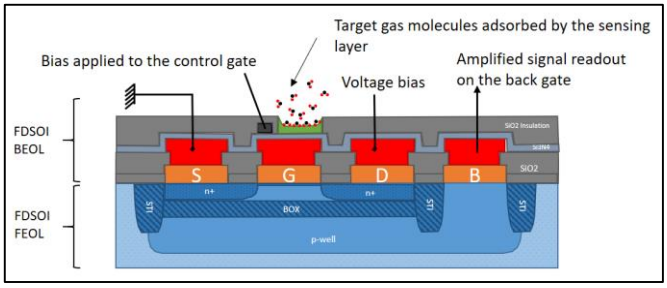

Fig.4: Cross-section view of the proposed Gas-FET sensor, showing the starting FDSOI front-end-of-line (FEOL) as well as the later layers integrated on the back-end-of-line of these transistors.

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Machine Learning Augmented TCAD Assessment of Corner Radii in Nanosheet FET

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Introduction: The amalgamation of modern computational learning tactics, such as deep learning, reinforcement learning, etc., with devices, may offer an implicit way to perform a cost and time-effective solution [1]. Recently, NSFETs have emerged as potential successors to FinFETs owing to their excellent gate controllability and increased effective width per footprint area [2]-[3]. One prime challenge in NSFET fabrication is the reliability of each sheet/stack. Even slight variations in sheet geometry, mainly the corners, significantly impacted the device characteristics. Sharp corners can lead to localized electric field crowding, thereby increasing leakage current and reducing reliability [4]. Thus, a faster and more efficient approach is needed for the variability analysis.

TCAD Setup and Machine Learning Model: Sentaurus TCAD [4] is used to simulate a single stack three-sheet NSFET as a baseline reference (Fig.1a-b). The simulation setup is calibrated against the experimental data [5] (Fig.1c). The TCAD setup includes a drift-diffusion and quantum potential model for carrier transport. The thin layer and high field saturation mobility models for governing the mobility degradation in thin sheets. The Auger and SRH models for carrier recombination, K. P model for energy band shift, etc., are included. Machine learning (ML) model is designed using the XGBoost algorithm for supervised learning. The root mean square error (RMSE) is used as a loss function for optimum accuracy. For data augmentation, the stacked autoencoder with InfoGANs is employed to generate the data that follows the original data distribution by maximizing the mutual information.

Results and Discussion: This paper proposes an ML approach to assist the TCAD results in realizing a local time-effective simulator for analyzing the vertically stacked Nanosheet FET (NSFET) performance metric. The corners are responsible for field crowding inside the sheets, significantly affecting the parasitic capacitance and reducing the I_{ON}/C_{gg} ratio. Thus, a detailed insight into corner radii optimization is being done. Using well-calibrated TCAD models, we demonstrate the corner rounding effect in Nanosheet FET and provide a possible design guideline for optimum DC/RF performance. The TCAD data is used in training the ML model, i.e., XGBoost regressor. The obtained RMS error is around 5.082×10^{-7} concerning 500 testing samples and 5.299×10^{-7} with unseen data. Further, the data augmentation technique is proposed using InfoGAN to suppress data imbalance and enhance the model accuracy. Thus, Machine learning augmentation with TCAD assessment is worth exploring to achieve a time-efficient solution for device simulation, fault prediction, and optimization.

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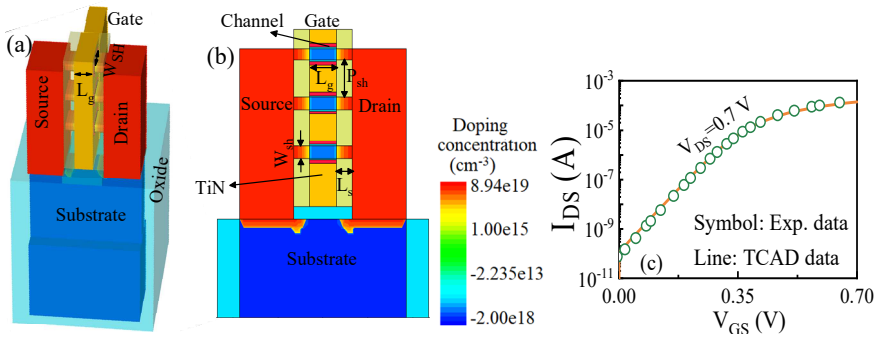

Table 1: Device Parameter

Parameter	Value
Gate length (L_g)	12 nm
Eff. oxide thick.	0.9 nm
Extension (L_{SP})	5 nm
Sheet Thickness	5 nm
Sheet Spacing	11 nm
Source/drain (S/D) doping	10^{20} cm^{-3}
Channel doping	10^{16} cm^{-3}

Fig. 1: (a-b) A three-stacked Nanosheet FET as a baseline NSFET; (c) TCAD model calibration against the experimental data [7]. Table-I comprises the parameters used in the simulation.

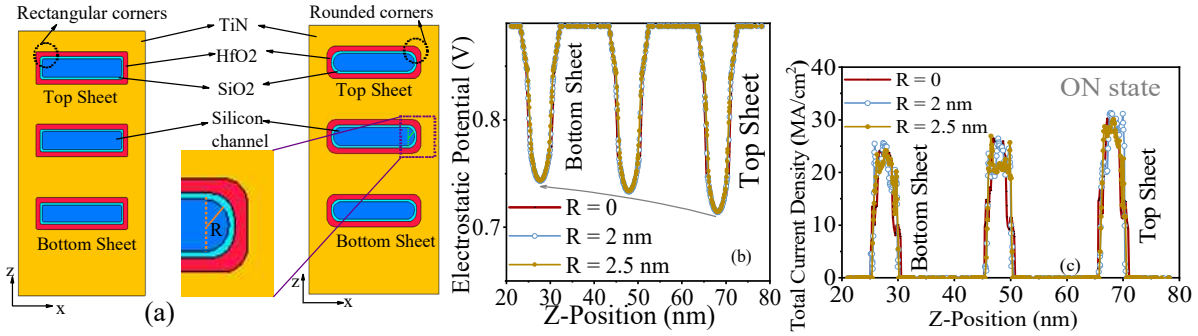

Fig. 2: (a) Cross-sectional view (along the x-z axis) of NSFET for a rectangular and rounded corner. The plots are drawn for different sheets, and the cutline is taken at the corner surfaces: (b) electrostatic channel potential; (c) electric field; (d) ON state current density.

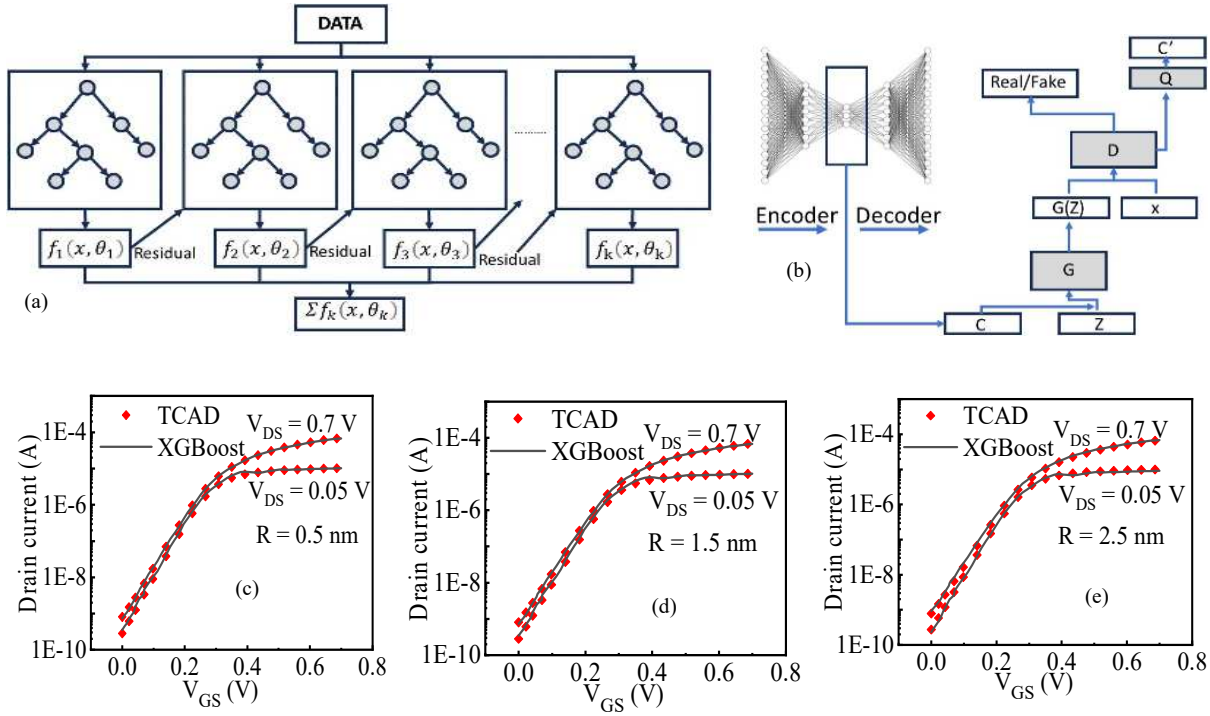

Fig. 3: (a) XGBoost used as a regressor. The boosting rounds have been set to 100, the learning rate to 0.1, and the max depth to 3; (b) InfoGAN architecture: generator architecture: 256, 128, 64, 32 dense, respectively; discriminator architecture: 256 & 128 dense; SAE architecture: 128, 64, 32, 5 dense (latent codes), 32, 64, 128 dense, respectively. (c-e) Model calibration with TCAD data.

Optimization and application of HiPIMS hafnium oxynitride (HfO_xN_y) thin films in MOS structures

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Several high-*k* materials, including metal oxides, nanolaminates, and silicates, are intensively studied for potential applications for high-performance or low-power Complementary Metal-Oxide-Semiconductor (CMOS) devices [1]. However, the crystallization temperature of HfO_2 is relatively low, leading to the growth of grain boundaries, which are perfect paths for oxygen, boron, and other impurities penetration into the semiconductor/dielectric interface [2]. One possible solution to improve insulating properties and increase crystallization temperature is nitrogen incorporation into the Hf-based high-*k* layer to form hafnium oxynitride (HfO_xN_y) [3]. This work's main aim was to develop the technology of thin hafnium oxynitride layers employing the High-Impulse Power Magnetron Sputtering (HiPIMS) method with improved electrical parameters. The optimization procedure was implemented using the Taguchi orthogonal tables. During the optimization procedure, the parameters of examined dielectric films were monitored employing optical methods (spectroscopic ellipsometry and refractometry), electrical characterization (C-V and I-V measurements of MOS/MOSFET structures), and structural investigations (AFM, XRD, XPS). The thermal stability of fabricated HfO_xN_y layers up to 800°C was also examined. The presented results have shown the correctness of the optimization methodology as HfO_xN_y layers formed using optimal HiPIMS process are characterized by improved electrical parameters, which is revealed in lower flat-band voltage (V_{fb}) values, the disappearance of frequency dispersion of C-V characteristics (Fig. 1), reduced effective charge (Q_{eff}/q), and interface traps (D_{itmb}) densities of examined MOS structures (Fig. 2). It is worth underlying that the improved electrical properties can correlate with the lower nitrogen content in the layer bulk and at the semiconductor-dielectric interface (Fig. 3). Moreover, the superior stability of HfO_xN_y layers up to 800°C was proved. Moreover, electrical properties or surface morphology deterioration has not been noticed. However, a slight increase of crystalline phase in the layer bulk was observed. The examinations of HfO_xN_y layers revealed comparable electrical properties (Fig. 4) and higher immunity to thermal treatment of dielectric films formed using HiPIMS compared to the standard Pulsed Magnetron Sputtering (PMS) technique (Fig. 5). Finally, we successfully applied HiPIMS HfO_xN_y films as gate dielectric films in MOSFET devices. The fabricated structures revealed improved electrical properties compared to FET structures based on silicon dioxide (SiO_2) gate dielectric layers (Fig. 6).

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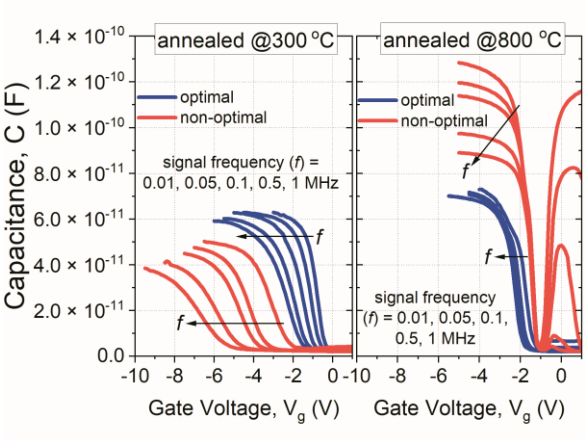

Fig. 1. Comparison of C-V characteristics of MOS structures with HfO_xN_y films fabricated using designed sets of parameters of reactive magnetron sputtering processes, i.e., optimal and non-optimal processes.

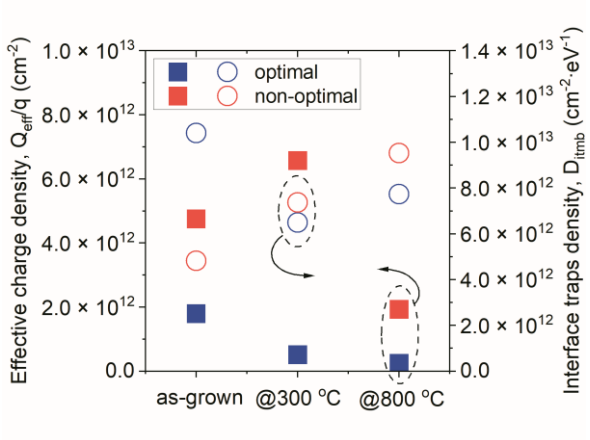

Fig. 2. Q_{eff}/q and D_{itmb} values estimated from the C-V characteristics analysis of MOS devices with HfO_xN_y as the gate dielectric film fabricated employed optimal and non-optimal HiPIMS processes.

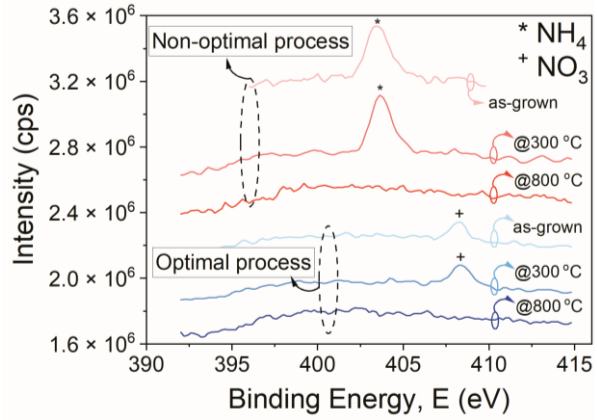

Fig. 3. N1s photoelectron spectra of investigated in this study HfO_xN_y thin films (as-grown and annealed at 300°C or 800°C).

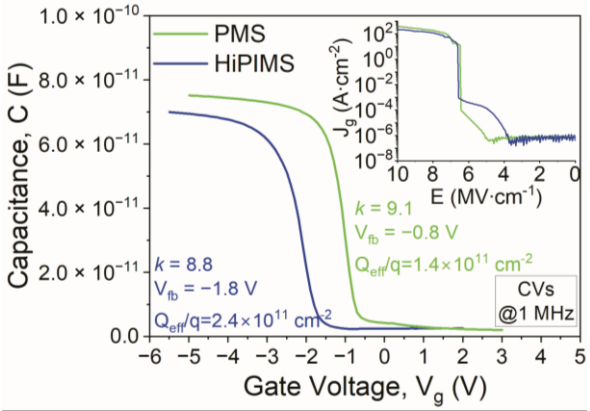

Fig. 4. Comparison of C-V characteristics of MOS devices with HfO_xN_y films fabricated using PMS and HiPIMS processes and annealed at 800°C; the inset shows the leakage current density vs. breakdown electric field intensity (E_{br}) of MOS structures.

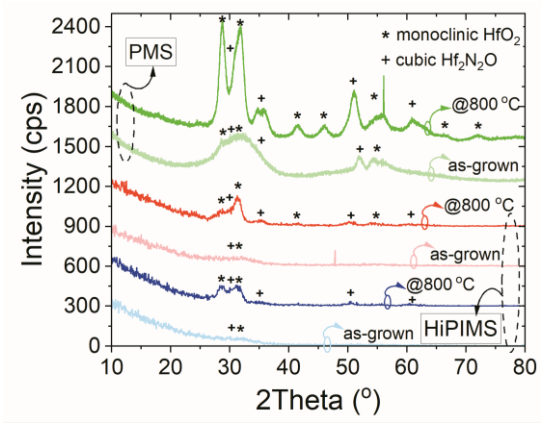

Fig. 5. Comparison of GIXRD patterns of dielectric thin films (as-grown and annealed at 800°C) fabricated using PMS and HiPIMS processes.

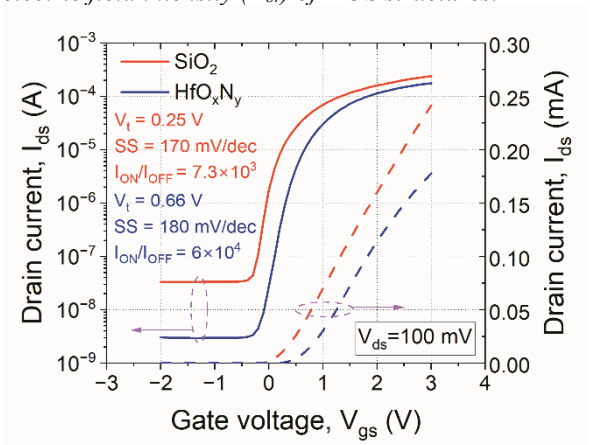

Fig. 6. Transfer characteristics of FET devices with thermal SiO_2 and HiPIMS HfO_xN_y layers (both 15 nm).

Reliability Aspects of Negative-Capacitance Stacked Nanosheet FET Considering Self-Heating Effect

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Abstract

This work investigates the impact of the negative capacitance (NC) effect on the performance of stacked nanosheet field-effect transistors (NSFETs), considering the influence of the self-heating effect (SHE). NC-NSFETs exhibit higher drain current (~21.4%) and improved transconductance compared to conventional NSFETs. The subthreshold swing (SS) of NC-NSFETs is lower than that of conventional NSFETs by ~3 mV/dec, indicating a steeper transition between the ON and OFF states. However, SHE reduces the drain current and transconductance of NC-NSFETs by reducing the mobility of charge carriers. It also degrades the SS of NC-NSFETs by increasing the scattering of charge carriers. The gate capacitance of NC-NSFETs is ~30.7% higher than that of NSFETs due to the presence of the ferroelectric layer. Investigation on static performance through inverter demonstrates that NC-NSFETs hold steeper voltage transfer characteristics comparatively and hence offer a higher noise margin among the considered configurations due to the large (~4×) I_{ON}/I_{OFF} ratio of NC-NSFETs.

Introduction

As semiconductor technology advances and transistors continue to shrink in size, new challenges arise in maintaining performance and efficiency. Beyond the 100 nm node, the formidable challenge of Short Channel Effects (SCE) emerges as a significant impediment. Drain-induced barrier lowering (DIBL) and subthreshold swing (SS) are identified as SCE factors that pose a substantial threat to device performance. The degradation of SS due to decreasing channel length results in an increment of I_{OFF}. The exploration of steep SS devices becomes imperative to address these challenges and ensure that VDD and Vth scale proportionally with transistor dimensions without causing a significant IOFF increment. Negative capacitance Field-Effect Transistors (FETs) emerge as a promising solution, offering the potential for steep SS devices **[1]-[3]**.

Results and Discussion

Numerical simulations are performed using Sentaurus 3D-TCAD of Synopsys Inc. for the targeted device **[4]**. The simulation deck is well-calibrated against the experimentally reported data on NSFET. The reliability of simulations is calibrated against experimental work reported in **[5]**, as shown in [Fig 1].

A) Impact of self-heating effect on device performance

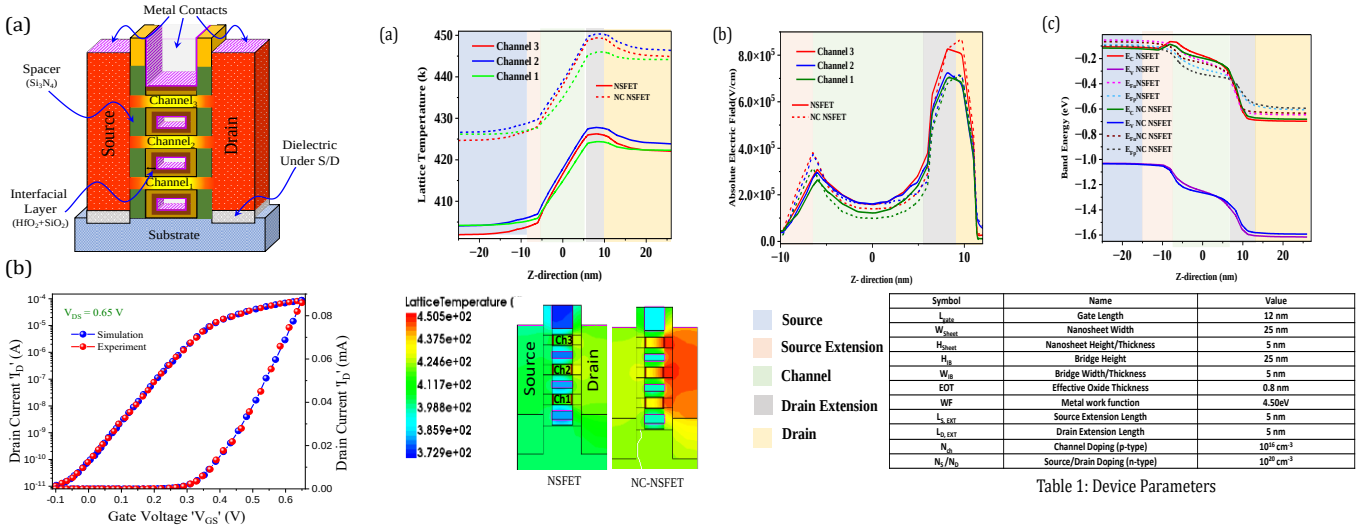
The Lattice Temperature, electric field, and band gap variations of the device are investigated [Fig 2]. NC-NSFETs exhibit a 21.4% enhancement in drain current compared to conventional NSFETs [Fig.3]. This is because the negative capacitance effect amplifies the gate voltage, which leads to a stronger inversion layer and higher channel conductivity. However, the self-heating Effect (SHE) degrades performance in both devices (~13.4% for NC-NSFETs, ~13.8% for NSFETs) [Fig.3]. The higher transconductance of NC-NSFET is due to higher channel conductivity, which shows a decrement of (~29.64%) due to SHE [Fig.4]. The ferroelectric material in the gate stack has a temperature-dependent polarization, which means that its negative capacitance decreases with increasing temperature. At a gate voltage of 0.6 V, the transconductance is higher as the temperature of the device is relatively low, which results in a high negative capacitance [Fig.4]. NC-NSFET exhibits a slightly higher threshold voltage (0.43 V) compared to the conventional NSFET (0.41 V) [Fig.5]. The subthreshold swing (SS) of NC-NSFETs is lower than that of conventional NSFETs. This means that the drain current changes more rapidly with VGS. The gate capacitance of NC-NSFET is greater than NSFET (~30.7%) and this capacitance remains relatively stable even with SHE. [Fig.6]. The I_{ON}/I_{OFF} of NC-NSFET (4.15×10^{7}) is better without a self-heating effect [Table 2].

B) Impact of self-heating effect on circuit performance

Inverters using NC-NSFETs demonstrate superior performance compared to their NSFET counterparts due to higher output voltage and steeper slope observed in the VTC curves [Fig 7]. Although the self-heating effect leads to a mild performance degradation, NC-NSFET inverters maintain their advantage. Notably, NC-NSFET inverters exhibit a significantly larger noise margin (NM), highlighting their greater tolerance to noise, which is crucial for reliable operation in environments with high noise levels. The specific NM values for NC-NSFET inverters without self-heating are NM_H= 0.3216 V and NM_L= 0.32 V, both higher than those observed in NSFET-based inverters [Table 2].

Conclusion

NC-NSFETs have demonstrated superior electrical characteristics compared to NSFETs. NC-NSFETs exhibit higher drain current (~21.4%), lower subthreshold swing (~3 mV/dec improvement), and higher transconductance, making them promising candidates for high-performance applications. Though the presence of the self-heating effect (SHE) is more significant in NC-NSFET, it holds a higher ON current, transconductance, and improved subthreshold swing compared to NSFETs. NC-NSFET also offers a higher noise margin, making it more suitable for digital applications.



Symbol	Name	Value
L_{gate}	Gate Length	12 nm
W_{Sheet}	Nanosheet Width	25 nm
H_{Sheet}	Nanosheet Height/Thickness	5 nm
H_{IB}	Bridge Height	25 nm
W_{IB}	Bridge Width/Thickness	5 nm
EOT	Effective Oxide Thickness	0.8 nm
WF	Metal work function	4.50eV
L_{S_EXT}	Source Extension Length	5 nm
L_{D_EXT}	Drain Extension Length	5 nm
N_{ch}	Channel Doping (p-type)	10^{16} cm^{-3}
N_S/N_D	Source/Drain Doping (n-type)	10^{20} cm^{-3}

Table 1: Device Parameters

Fig. 1. (a) 3D NSFET, and **(b)** calibration of the used models against fabricated NSFET.

Fig. 2. (a) Lattice temperature variation due to self-heating of devices. **(b)** Electric field variation along the x-axis due to SHE. **(c)** Bandgap of the devices due to SHE. **Table 1:** Device Parameters.

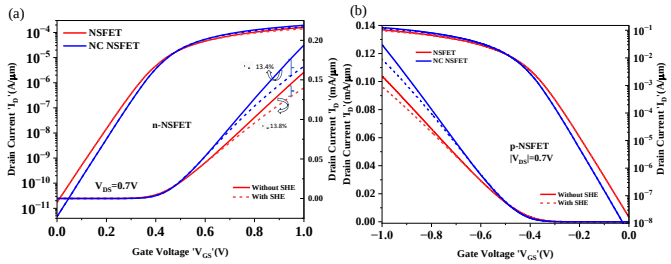


Fig. 3. a) I_{DS}–V_{GS} comparison between n-NSFET and NC-NSFET with and without SHE. **b)** I_{DS}–V_{GS} comparison between p-NSFET and NC-NSFET with and without SHE.

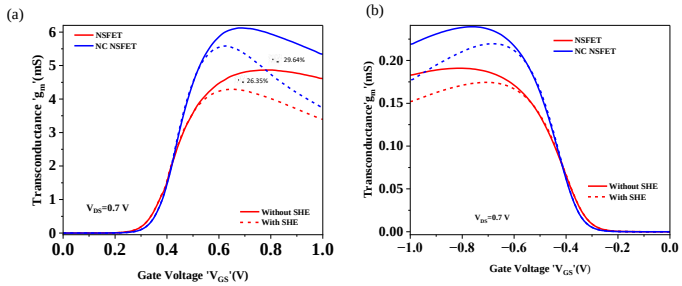


Fig. 4. a) g_m–V_{GS} comparison between n-NSFET and NC-NSFET with and without SHE. **b)** g_m–V_{GS} comparison between p-NSFET and NC-NSFET with and without SHE.

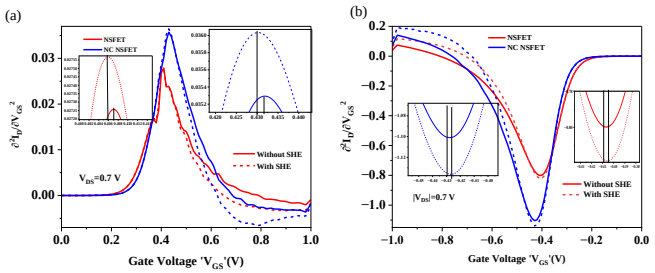


Fig. 5. a) Threshold voltage comparison between n-NSFET and NC-NSFET with and without SHE. **b)** Threshold voltage comparison between p-NSFET and NC-NSFET with and without SHE.

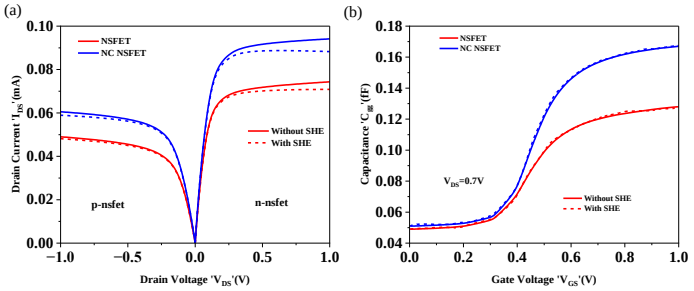


Fig. 6. a) I_{DS}–V_{DS} comparison between NSFET and NC-NSFET with and without SHE. **(b)** Capacitance vs V_{GS} comparison between n-NSFET and NC-NSFET with and without SHE.

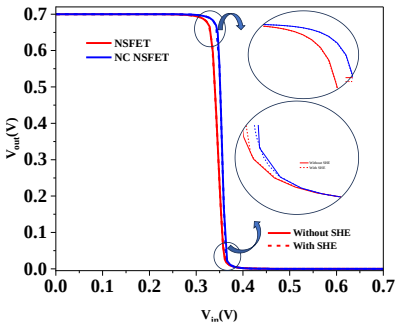


Fig. 7. Voltage Transfer Characteristics of an inverter using NSFET and NC-NSFET with and Without SHE.

Table 2: Results

Device	I_{OFF} (A)	I_{ON} (mA)	SS (mV/dec)	I_{ON}/I_{OFF}	NM_L(V)	NM_H(V)
NSFET W/O SHE	$2.88x10^{-10}$	2.66	67.59	$9.24x10^{6}$	0.2	0.3157
NSFET W/I SHE	$2.88x10^{-10}$	2.33	67.61	$8.09x10^{6}$	0.1897	0.3163
NC NSFET W/O SHE	$7.78x10^{-11}$	3.23	64.46	$4.15x10^{7}$	0.3216	0.32
NC NSFET W/I SHE	$7.78x10^{-11}$	2.78	64.478	$3.57x10^{7}$	0.3196	0.3151

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Performance Optimization of III-V Homo/Heterojunction Line TFET: Device-Circuit Interaction

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Abstract
In this work, we optimize the parameters of the epitaxial layer (N_{epi}, T_{epi}) gate overlap length and L_{ov} for the n-type InGaAs homojunction III-V Line tunnel field effect transistor (L-TFET). The L-TFET with small bandgap III-V materials gives a high ON current and steep subthreshold slope with less power consumption. This improvement in the device performance is due to the small bandgap of the III-V materials. The optimized values of Lov, N_{epi}, and T_{epi} are 4nm, 1×10^{19} cm^{-3}, and 20nm, respectively. The optimized parameters are used for designing other III-V (homo/heterojunction) L-TFETs, and it found that the performance of GaAsSb/InGaAs heterojunction L-TFET is better in terms of I_{on}/I_{off} ratio, transconductance (g_m) and subthreshold swing (SS). We have designed the inverter using n-type and p-type InGaAs homojunction and GaAsSb/InGaAs heterojunction L-TFETs to analyze the voltage transfer characteristics (VTC) and transient response of the inverter.

Introduction
The use of IoT and automation technologies has raised the requirement for energy-efficient equipment. Energy-efficient devices often use V_{DD} scaling. Boltzmann's tannery in sub-30nm CMOS inhibits supply voltage scaling. Researchers are exploring new MOS device designs and materials to exceed Boltzmann's 60mV/decade barrier. L-TFETs have a p-i-n gated configuration similar to MOSFETs and are compatible with current production procedures. L-TFET conduction involves mostly quantum mechanical band-to-band tunneling (BTBT). Si, Ge, SiGe, and low bandgap (III-V) materials such as InGaAs, InP, GaAsSb, etc., may improve L-TFET device performance [1]. Low-bandgap III-v L-TFETs have reduced power consumption, a smaller bandgap, better tunneling generation, and less lattice mismatch and interface traps.

Simulation Methodology
We employ InGaAs in the source, drain, channel, epitaxial layer, and substrate areas in homojunction InGaAs L-TFET device structure in [**Fig. 1(a)]**. The spacer material is chosen as high-κ HfO_2 to improve drain current and electrostatic control [2]. The material parameters employed in the simulation are presented in **Table I** [3]. The device [2], [4] and material [3] calibration with experimental data shows a good match in [**Fig. 1(b-c)]** using Sentaurus TCAD [4]. We have employed WKB approximation and nonlocal BTBT models at all possible tunneling junctions, along with the Philips mobility model, Shockley-Read-Hall (SRH) recombination, Schenk TAT models for trap-assisted tunneling, and the Old-Slotboom bandgap narrowing model for spacer region carrier density **Table-II**.

Results and discussion
Device simulation is performed to optimize the doping concentration (N_{epi}), thickness (T_{epi}) of the epitaxial layer and overlap length (L_{ov}) for the proposed $In_{0.53}Ga_{0.47}As$ homojunction L-TFET device. Increasing drain voltage leads to increased drain current in the L-TFET device as the density of states available for tunneling (occupancy probability) increases **[Fig. 2]**. A near-perfect saturation is observed in the output characteristics of the proposed device, which in turn provides high output resistance.

A. Optimization of Homo/Hetero Junction III-V L-TFET
Optimization of N_{epi} is done considering lower I_{OFF}, as the OFF current starts increasing due to the thinning of the potential barrier between the source and epitaxial layer **Fig. [3**]. While T_{epi} optimized for higher I_{ON} along with I_{OFF}, as OFF current increases linearly and control of the gate at the tunneling junction is lost at more T_{epi} **Fig. [4**]. For optimization of L_{OV}, there is no change in tunneling length and tunneling width with L_{OV}, which is primarily due to the increase in the effective cross-section area for tunneling at source epitaxial layer junction **Fig. [5**]. The current increases almost linearly with L_{OV} and this can be used as a circuit design parameter. Device band bending happens with the variation of these physical parameters (Lov, N_{epi}, and T_{epi}) along with the electric field. The I_{on}/I_{off} current ratio of this device is 1.88×10^{10} **Fig. [3-5**]. Although not shown here, we have optimized the heterojunction III-V (GaAsSb/InGaAs) L-TFET similarly.

B. Material Optimization for Heterojunction III-V L-TFET
The InP/InGaAs hetero and InGaAs homo structures optimization give similar device parameters. The epitaxial region made up of small bandgap material gives a high tunneling rate so that it gives more drive current [3]. The g_m of hetero L-TFET is more than homo L-TFET because hetero L-TFET has more I_{ON} than homojunction L-TFET **[Fig. 6]**. The C_{gd} is more than C_{gs}, as C_{gd} forms the miller capacitance. C_{gd} is the dominant capacitance since there is a less potential drop between the channel and drain and because tunneling between the source and epitaxial layer is less so as C_{gs} is less **[Fig. 7]**.

C. Comparison of Digital Performance using Inverter
We compared the performance of InGaAs homojunction and GaAsSb/InGaAs heterojunction L-TFET inverters **[Fig. 8]**. The VTC and transient response of InGaAs homojunction and GaAsSb/InGaAs heterojunction L-TFET-based inverters **[Fig. 9]**. The supply voltage is 0.5V, and the load capacitance is 1aF. The transient analysis assumes 1 ns delay, rise and fall times and 0.5V peak-to-peak voltage. The p-type L-TFET driving current should be improved by increasing source doping concentration. However, the source is very degenerate due to the low density of states in the conduction band, which might alter the subthreshold swing steepness. The transient response plot of the InGaAs L-TFET inverter shows a little overshoot. The miller capacitance (C_{gd}) of n and p-type L-TFETs causes it. Low bandgap and density of states characterise III-V materials. In GaAsSb/InGaAs L-TFET inverters, overshoot is absent. **[Fig. 10]** demonstrate the VTC of 0.3 V InGaAs homo and GaAsSb/InGaAs hetero L-TFET inverters. At 0.3V supply voltage, InGaAs homo and GaAsSb/InGaAs hetero L-TFET-based inverters display transient responses. The VTC charts of both inverters show that they function similarly at 0.3 V and 0.5 V supply voltages. InGaAs and GaAsSb/InGaAs L-TFETs may utilize lower supply voltages.

Conclusion
In this work, we have achieved the optimum performance of the InGaAs homojunction L-TFET with the optimized values of 1×10^{19} cm^{-3} N_{epi}, 20nm L_{ov}, and 4nm T_{epi}. The improvement in I_{ON} is 0.3 mA/μm, the I_{OFF} can be reduced to 2.48×10^{-13} A/μm, and the minimum SS is achieved as 14 mV/decade. Additionally, we optimized the GaAsSb/InGaAs hetero L-TFET, and we observed the same optimization parameters for the device. Altogether, we have compared different homo/heterojunction III-V L-TFETs with the same structure and specifications. GaAsSb/InGaAs heterojunction L-TFET performs better in terms of I_{on}/I_{off} and device SS. Finally, we have examined InGaAs homojunction GaAsSb/InGaAs heterojunction L-TFET based inverter performance, and we have observed a good noise margin for the heterojunction for nominal voltage and for near-threshold voltage, homojunction L-TFET a good choice for circuit application **[Table-III].**

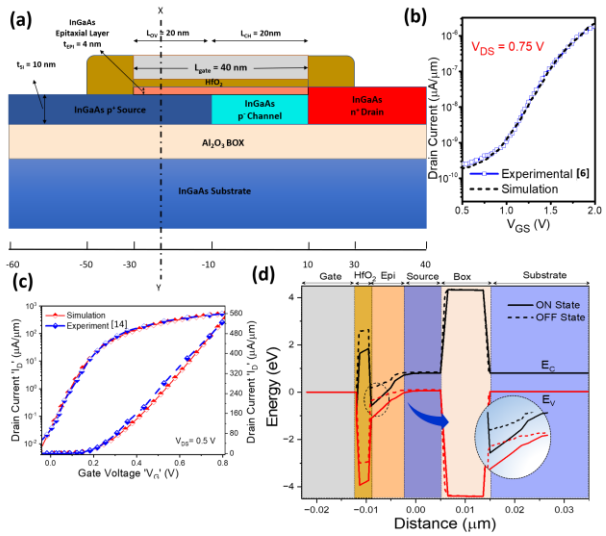

Fig. 1 (a) 2-D schematic of InGaAs homojunction L-TFET (b) Device calibration (c) InGaAs Material calibration (d) Band diagram of the device in on-state & off-state.

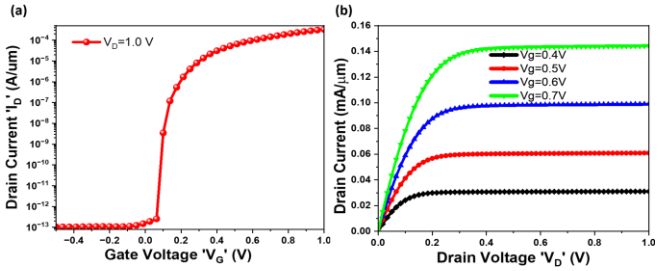

Fig. 2 (a) Transfer characteristics of InGaAs Homojunction L-TFET (b) Output characteristics of InGaAs Homojunction L-TFET.

Table I
Material Parameters **[3]**

Parameters	InGaAs	InP	GaAsSb
E_G (ev)	0.80	1.35	0.8215
Electron affinity	4.5eV	4.38eV	4.46eV
Electron tunneling mass (m_{tc})	0.043 m_0	0.08 m_0	0.08 m_0
Hole tunneling mass (m_{th})	0.052 m_0	0.012 m_0	0.089 m_0
Degeneracy (g)	2	2	1

Table II
Simulation Parameters

Symbol	Name	Value
L_{spacer}	Length of Spacers	20 nm
N_S	Source Doping (p-type)	5 x 10^{19} cm^{-3}
N_D	Drain Doping (n-type)	5 x 10^{18} cm^{-3}
N_{EPI}	Epitaxial Layer Doping (n-type)	1 x 10^{19} cm^{-3}
N_{ch}	Channel Doping (p-type)	10^{17} cm^{-3}

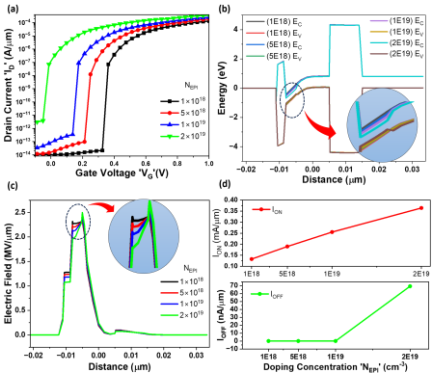

Fig. 3 (a) Transfer characteristics (b) Band diagram (c) Electric Field (d) on & off current at different doping concentrations of epitaxial layer (N_{EPI}).

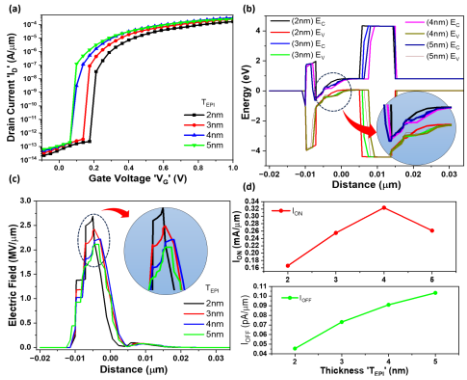

Fig. 4 (a) Transfer characteristics (b) Band diagram (c) Electric Field (d) on & off current at different thickness of epitaxial layer (T_{EPI}).

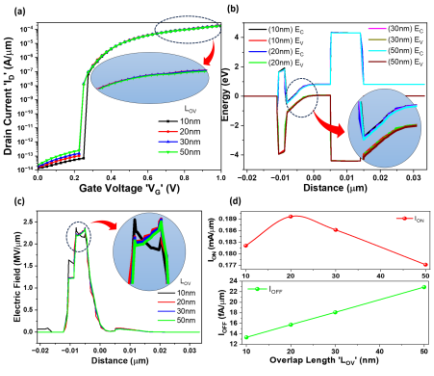

Fig. 5 (a) Transfer characteristics (b) Band diagram (c) Electric Field (d) on & off current at different overlapping lengths (L_{OV}) of the epitaxial layer.

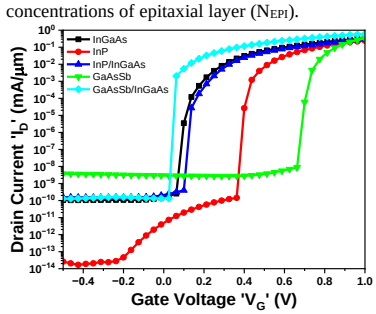

Fig. 6 Comparison of transfer characteristics of different III-V material-based L-TFETs.

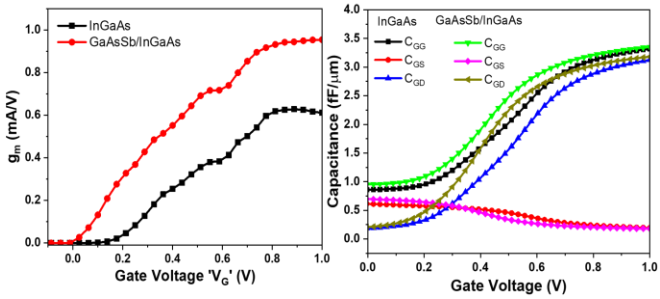

Fig. 7 (a) Transconductance (g_m) vs. gate voltage characteristics (b) capacitance vs gate voltage characteristics of InGaAs homo and GaAsSb/InGaAs hetero L-TFETs.

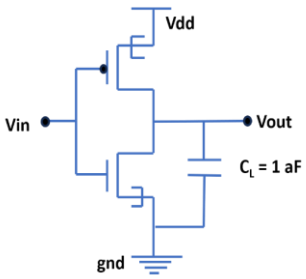

Fig. 8 Schematic of inverter.

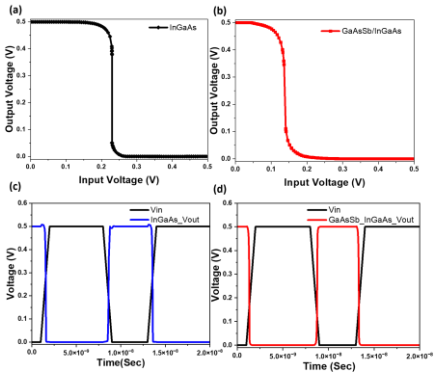

Fig. 9 VTC of inverter using (a) InGaAs & (b) GaAsSb/InGaAs L-TFETs and transient response of inverter using (c) InGaAs & (d) GaAsSb/InGaAs L-TFETs at 0.5 V supply voltage.

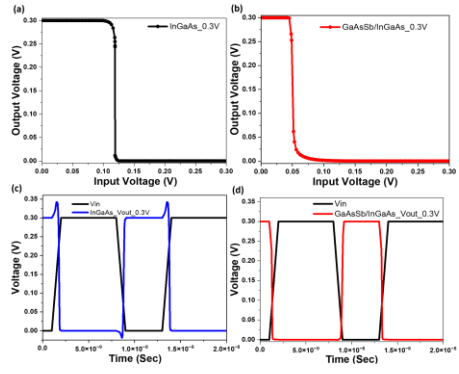

Fig. 10 VTC of inverter using (a) InGaAs & (b) GaAsSb/InGaAs L-TFETs and transient response of inverter using (c) InGaAs & (d) GaAsSb/InGaAs L-TFETs at 0.3 V supply voltage.

Table III
Parameters of Inverter with homo and hetero (InGaAs/GaAsSb) Junction.

	At 0.3 V Supply		At 0.5 V Supply	
Parameters	InGaAs	InGaAs/GaAsSb	InGaAs	InGaAs/GaAsSb
NM_H	0.18	0.0238	0.25	0.396
NM_L	0.11	0.0425	0.21	0.168
Rise Time	0.3ns	0.48 ns	0.13ns	0.27 ns
Fall Time	0.3ns	0.21 ns	0.06ns	0.18 ns

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A Planar Core-Shell Junctionless Transistor Compatible with FD-SOI Technology

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Junctionless (JL) transistors have gained interest for their simple fabrication and potential in 3D integration demanding low thermal budget [1]. The absence of lateral junctions improves reliability, short-channel effects and parasitic capacitance. However, to ensure reasonable output current, high doping concentration above 10^{19} cm^{-3} is suitable, resulting in poor mobility and normally-ON operation. Core-shell (CS) nanowire structure was proposed to solve the issues of JL transistors while maintaining their attractive features [2].

In this work, we propose a planar version of CS-JL FET, fully compatible with standard FDSOI process. The transistor looks like an A2RAM (inset Fig. 1) [3], except that the N^+ core is heavily doped and both the core and the shell are ultrathin (3-4 nm). Raising the gate voltage (V_G) first incites the carriers to fill the low-mobility core, approaching the maximum concentration governed by the nominal doping. Then, free carriers start to accumulate in the undoped shell and benefit of high mobility. Once in strong accumulation, the gate voltage is absorbed by the carrier population in the shell, hence the carrier concentration in the core is hardly changed. Note that the electron concentration is no longer limited by doping and only depends on the gate voltage over-drive.

Simulations with Sentaurus TCAD demonstrate the tremendous advantage of the CS-JL transistor over classical JL (Fig. 1). First, the threshold voltage is shifted from a negative value (normally ON) to a positive value (normally OFF). Second, the drive current is significantly higher due to mobility improvement. As a matter of fact, the transconductance is increased by one order of magnitude (Fig. 2a). The threshold voltage (V_{th}) of CS and JL transistors was extracted by the double derivative of the drain current (Fig. 2b) which exhibits two peaks. The first peak indicates V_{th} of the core and stands as the V_{th} of the CS-JL FET. The second peak gives the threshold voltage of the shell, as in a MOSFET, which is actually close to the flat-band voltage of the core. Split-capacitance curves are reproduced in Figure 3a. Their derivatives (Fig. 3b) also feature two peaks confirming the delay between the activation of the core and shell. Figure 3c shows the electron mobility extracted form capacitance and current characteristics. In the core-dominated conduction regime, the mobility is low, as in the reference JL, but suddenly increases as soon as the shell is activated, reaching typical values observed in FD-SOI MOSFETs. These characteristics demonstrate the superiority of the core-shell architecture in JL transistors envisioned for 3D sequential integration. We will discuss the impact of core doping and thickness on the performance in devices with gate length from 200 nm down to 20 nm.

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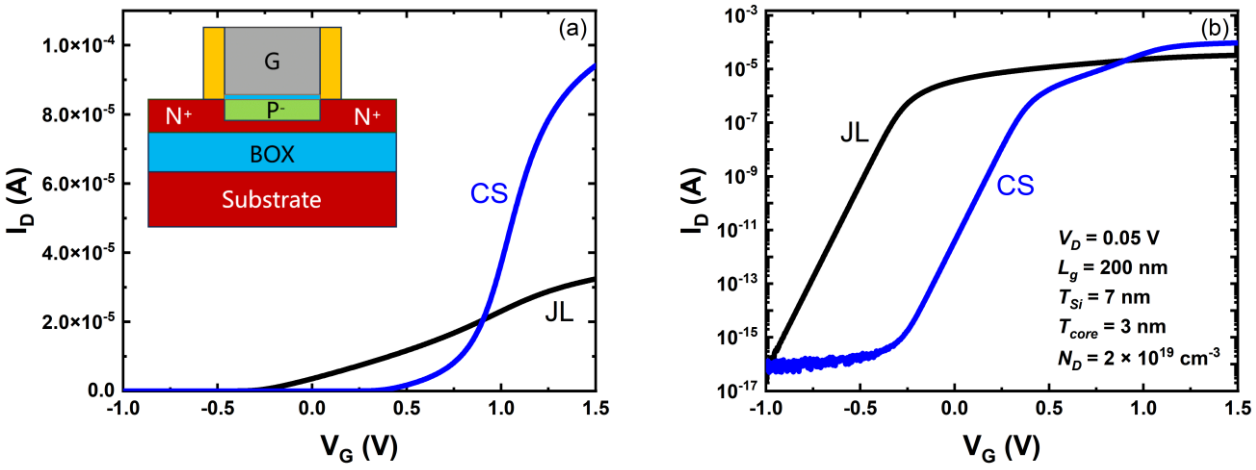

Figure. 1. Transfer characteristics of CS and JL FETs. (a) Linear scale and device architecture. (b) Semi-log scale.

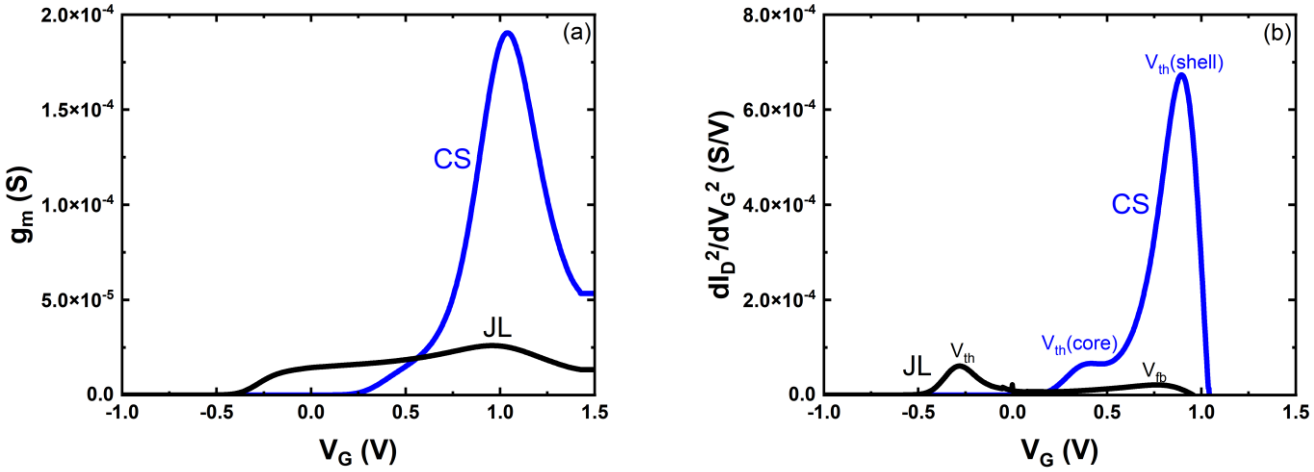

Figure. 2. Transconductance characteristics. (a) Transconductance versus gate voltage. (b) Double derivative of drain current versus gate voltage.

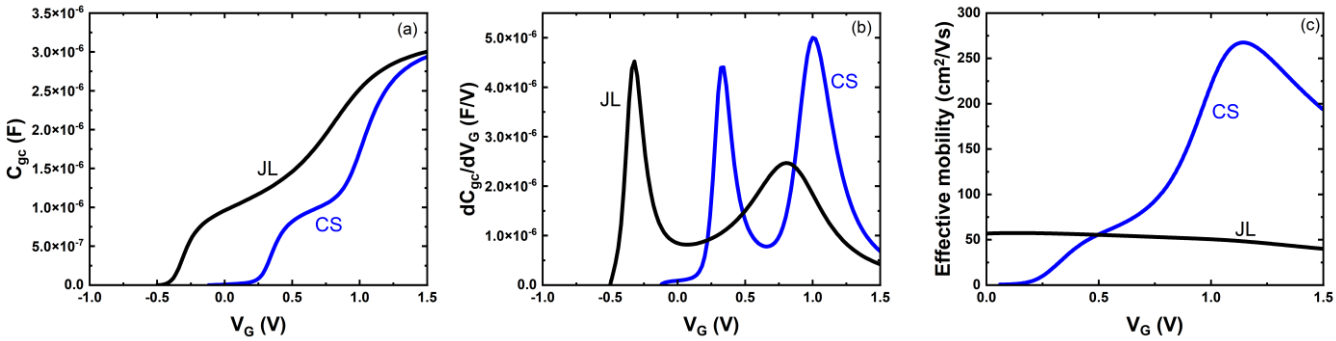

Figure. 3. (a) Gate-to-channel capacitance, (b) capacitance derivative and (c) electron mobility versus gate voltage. The mobility for CS is an average value combining the core and shell contributions.

New Insights into Back-Biasing Effects in Advanced FD-SOI MOSFET

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A unique feature of FD-SOI MOSFETs is back biasing. It is well known that applying forward ($V_{BG} > 0$ for n-type channels) and reverse ($V_{BG} < 0$) bias on the back gate enables the threshold voltage (V_T) to be adjusted for achieving high performance or low power consumption. In this paper, we also address less documented effects of back biasing: *DIBL*, mobility collapse, series resistance, etc. Simulations of 22nm node FD-SOI technology compare short and long n-channel MOSFETs featuring different ground plane doping (N^+ and P^+) and architectures.

The theoretical coupling factor, $\gamma = \Delta V_T/\Delta V_{BG} = -t_{ox}/t_{box}$, is unable to account for deviations observed in ultrathin transistors. Figure 1 shows that the accuracy of the coupling factor depends on the method used to extract the threshold voltage. Out of six techniques tested, the Y-function systematically underestimates the impact of coupling. The modified Y-function and the derivatives of transconductance and capacitance produce compatible results. The current reference method can also be reliable, provided the reference current is properly selected. Another issue is the calculation of γ, which requires the precise extrapolation of *EOT* from C-V characteristics. While the difference between long and short transistors is minor, SLVT (super low V_T by flip-well) devices feature a higher coupling than RVT (regular V_T with P^+ groundplane) counterparts. The coupling tends to be accentuated for positive V_{BG} due to volume inversion [1].

Volume inversion is also responsible for a degradation of the subthreshold swing (*SS*), in particular in short devices (Fig. 2a). When the electrons are confined near the top interface, *SS* and *DIBL* are reduced (Fig. 2b) but the mobility decreases significantly (Fig. 2c). Figure 3 shows how the back bias modifies the threshold voltage roll-off and the mobility collapse observed in transistors shorter than 70 nm. Note that the mobility can drop by 35% whereas the threshold voltage decrease is reasonable. Another intriguing aspect is the lowering of the series resistance for $V_{BG} > 0$ (Fig. 4), suggesting that electrostatic doping reinforces the physical doping of the terminals.

These various aspects are clarified by considering the profiles of carriers and electric field in the body. We will discuss the pragmatical trade-off between attenuated short-channel effects and boosted performance by back biasing, which is important for circuit design.

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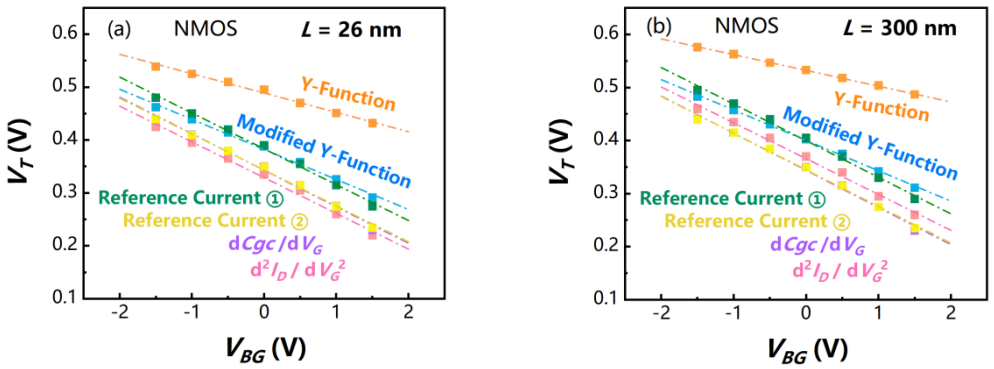

Figure 1. Different V_T extraction methods for (a) 26nm channel length and (b) 300 nm channel length FDSOI RVT nMOSFETs.

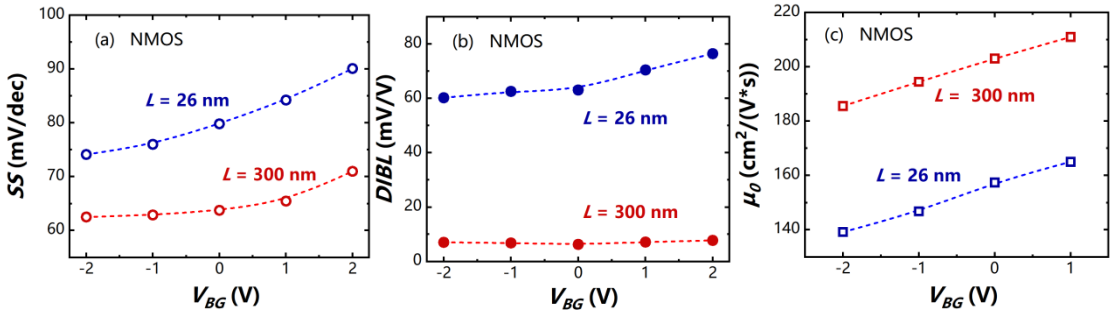

Figure 2. (a) Subthreshold swing *SS*, (b) *DIBL* and (c) zero-field mobility versus back voltage. RVT nMOSFETs with short and long channels.

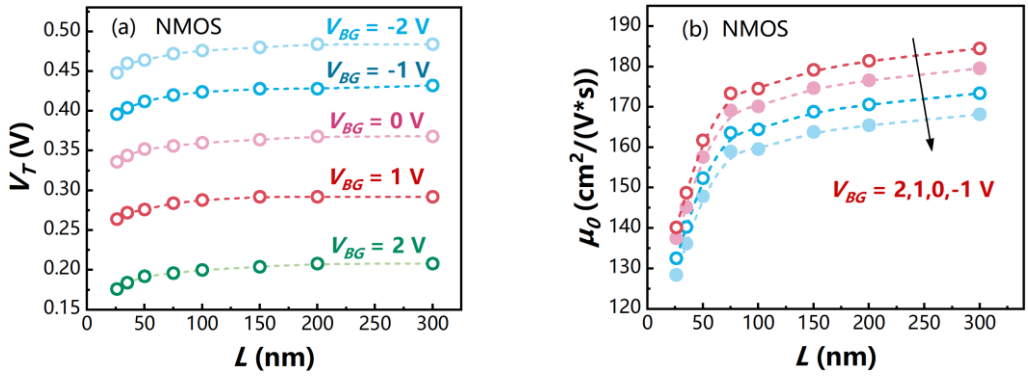

Figure 3. (a) V_T roll-off and (b) mobility collapse versus channel length for variable back bias in RVT nMOSFETs .

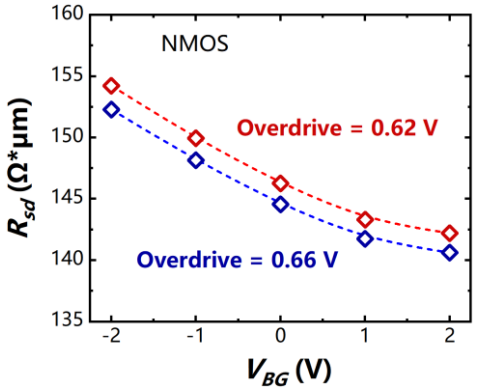

Figure 4. Series resistance variation with back voltage in RVT nMOSFETs .

Nanowire Behavior Under the Influence of Polyoxometalates: A Comparative Study of Depletion and Enhancement Modes

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Abstract— Polyoxometalates (POMs) are one of the most adaptable families of inorganic molecular materials due to the wide variety of shapes and properties they can exhibit. In this paper, we investigate polyoxometalates (POMs), whose notable redox properties entail the same behaviour, as prospective charge storage nodes as part of Si-nanowire transistors [1]. POMs are molecular metal oxides, composed of early transition metal ions and oxo ligands. POMs can be readily synthesized in solution from their simple metal oxides [2]. Fig. 1 demonstrates one such example of an optimized geometry of a non-classical Wells–Dawson anion, [W18O54(SO3)2]4-. Fig. 2 illustrates the configuration of a FinFET device in the simulation domain, including the presence of POMS molecules and other material layers. The Si NW FinFETs were fabricated on a silicon-on-insulator (SOI) substrates with a top Si layer of 55 nm and a buried oxide thickness of 150 nm. The cross-sectional scanning electron microscope (SEM) image in Fig. 3 shows the distinct sources, drain, and gate areas of the device, as well as the bond pads used for making contacts. The processed silicon nanowire structure with 200 nm gate length is used for this analysis and designed in the sentaurus device editor (SDE) and further electrostatic study has been performed using the Synopsys TCAD simulator [3]. We investigated the relationship between device operation and sensitivity with respect to the mode of operation i.e. depletion and enhancement mode. Drain Induced Barrier Lowering (DIBL) has been performed to see the effect of the short channel effect (SCEs) and presented in Fig. 4 for both operational modes. Furthermore, we simulate the POMS molecule as a negatively charged volume, allowing us to study its effect on the silicon surface. Charge on the device when placed on the surface at the center causes an abrupt shift in the electric field and electrostatic value at the position of the POMS molecule. We found the electric field increases from 1.95 $MVcm^{-1}$ to 1.99 $MVcm^{-1}$ and the electrostatic potential changes from 1.04 V to 0.90 V at the place of the molecule as shown in Fig. 5. Next, we focus on the effect of the position of the POM molecules on the nanowire transistor. We performed this study for both depletion mode (DM) and enhancement mode (EM) of operation. Since the electron density beneath the gate increases at varying positive gate bias due to the inversion process of the MOS capacitor in EM, the percentage change in electron density is more significant in EM than in DM as shown in Fig. 6. Our simulation work reported here provides design rules for fabricating the optimized device geometry with improved performance to be used for sensing applications in molecular based electronic devices.

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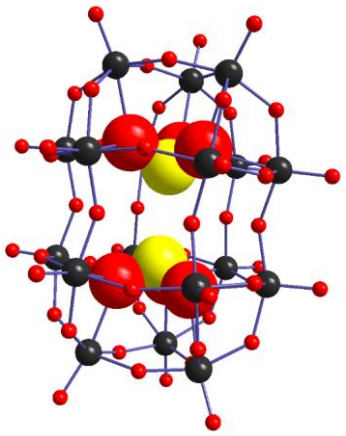

Figure 1. An example of a non-classical Wells–Dawson anion, [W18O54(SO3)2]4-. This geometry was optimized using DFT, utilizing the ADF package of the Amsterdam Modelling Suite.

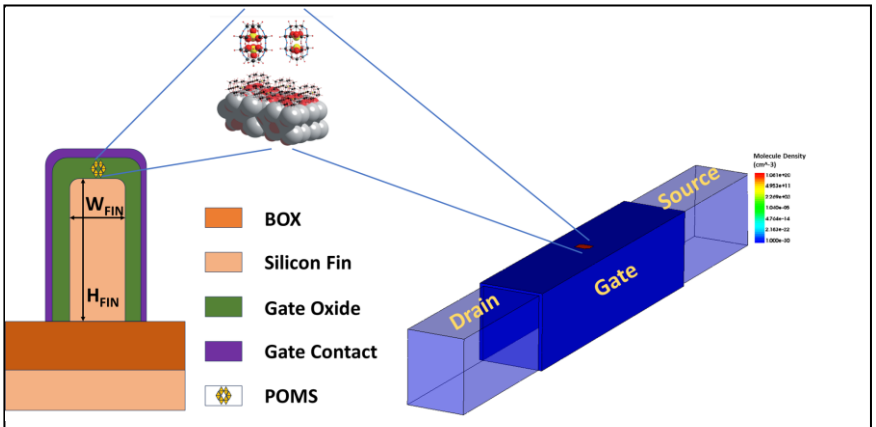

Figure 2. Two dimensional cross section view (right) of the Silicon Fin and Three dimensional camera view (left) with the position of the POMS molecule

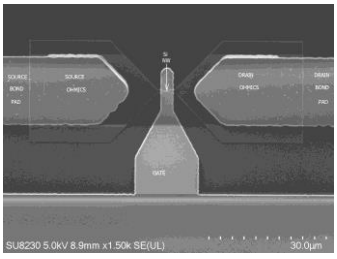

Figure 3: Cross-sectional SEM image of device depicting different sources, drain and gate regions along with the bond pads to make contacts.

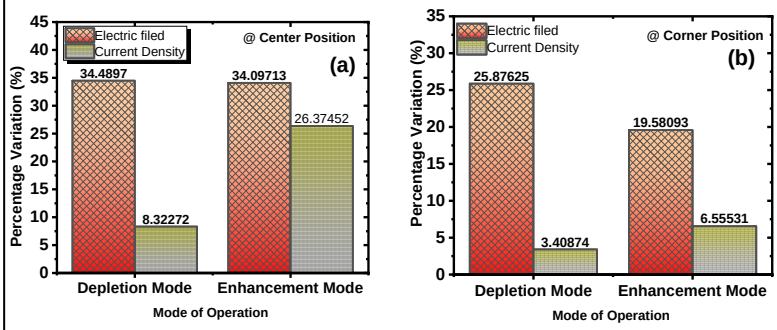

Figure 6: Percentage variation on the absolute value of the electric field and current density for the depletion and enhancement mode of operation due to the presence of the POMS molecule on the device at (a) center position and (b) corner position.

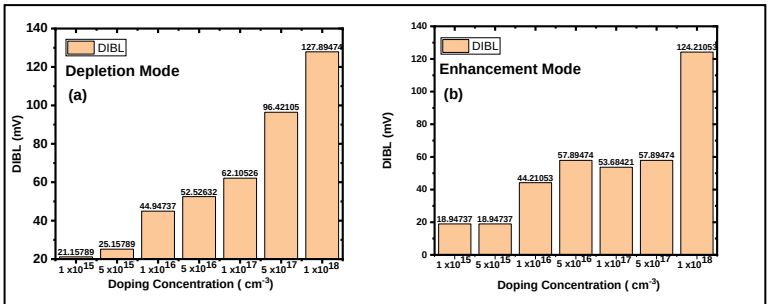

Figure 4: Impact of the DIBL variation due to doping concentration of the channel region for the (a) Depletion and (b) Enhancement Mode of operation.

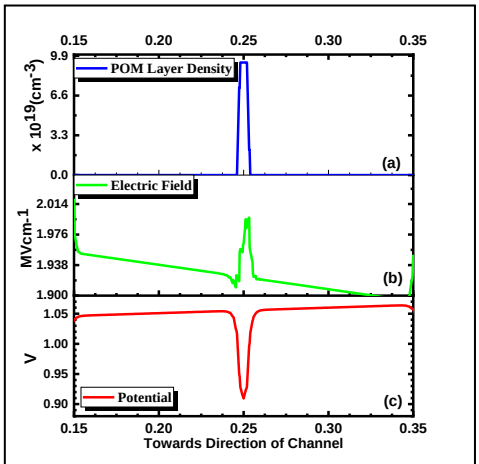

Figure 5: Variation of the (a) charge density, (b) electric field, and (c) potential across the channel direction due to the presence of the POMS molecule on the surface at the centre of the device.

Optimizing Peptide Detection Using FET-Based Sensors: Integrating Non-Linearities of Surface Functionalization

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Abstract: This study presents a method for enhancing peptide interaction with ATPES/linker, utilizing tert-Butyloxycarbonyl to protect the N-terminal and prevent undesirable reactions. Addressing noise interference in peptide recognition, we devised a noise-filtering technique that enables accurate peptide signature retrieval even at low signal-to-noise ratio (SNR) by leveraging the full pH titration spectrum. Additionally, our research explores the impact of BOC protection levels on the functionalization of amine surfaces with APTES, highlighting how silanol sites influence the isoelectric point, surface potential, and capacitance. These findings underscore the necessity of considering chemical protection and surface chemistry in peptide synthesis and sequencing, offering valuable insights for bioanalytical applications.

Results and Discussion: For selective interaction of peptides with the ATPES/Linker, N-terminal is protected with tert-Butyloxycarbonyl (BOC) to prevent unwanted protonation or interaction with other molecules (organic/inorganic) [1] [Figure 1]. The designed BOxSim module is used to study the BOC deprotection with the effectiveness of N-terminal of APTES to interact with the electrolyte at different pH conditions [2]. Along with the BOC quantification, Noise can affect both the recognition of fingerprints as the fast variations perturb the recognition of singularities in the derivates of the signal and the recognition of peptides. For this reason, we have developed a methodology to filter the noise. Figure 2(c) shows the extracted signal, which corresponds 100% with the analytical model. In this way, we have shown that it is possible to retrieve the peptide signatures even with SNR < 10dB if the complete titration spectrum of pH can be accessed [3]. Figure 3 shows the calculations for an amine surface (APTES functionalization) with different degrees of BOC surface, first with 100% amine functionalization and with the contribution of silanol groups in the case of practical functionalization (Figure 4). In the presence of silanol sites [10%], the isoelectric point varies from approx. 4 to 10 as the BOC-deprotection increases from 0% to 99% of the total surface states [Figure 4(a)] [4]. As the device width and resistivity are the same for simulation results of Fig. 3 and 4, the drain current range also remains the same but with the change in surface potential [5], the drain current [Fig. 3(d) and 4(d)] varies with respect to the bulk pH keeping the second derivative with the same zero-crossover points. Thus, at any constant current, the variation of reference bias will follow the surface potential of that specific device with different parameters.

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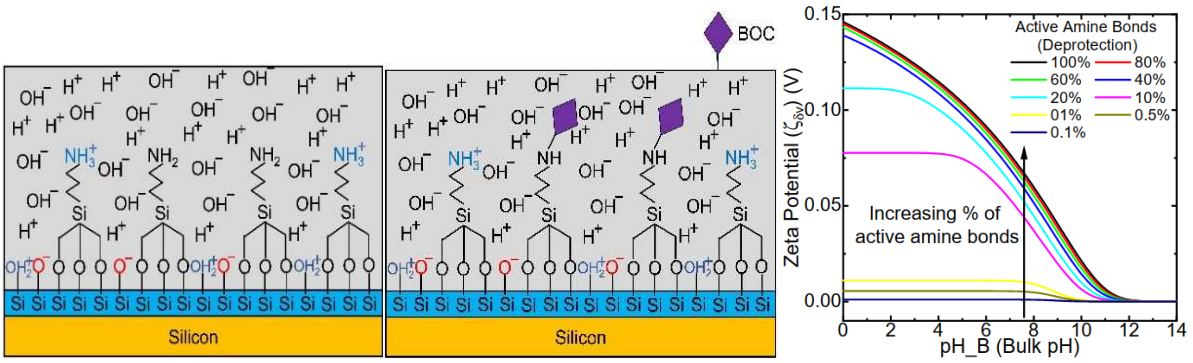

Fig. 1. (a) Schematic of FET-Sensor's surface interaction with electrolyte in the presence of (a) APTES (b) APTES protected with BOC along with Silanol sites (b) Zeta potential variation with different percentages of BOC

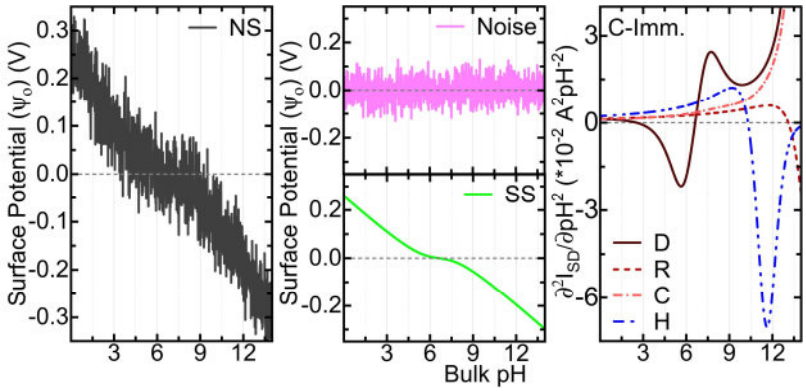

Fig. 2. (a) Simulation of noisy Ψ_o vs. pH signal with SNR=10dB; (b) Extracted Noise; (c) Extracted clean signal (d) Extracted Ψo vs. pH signal from (a) for Carboxy-terminal immobilized aspartic acid; (d) second order gradient of Drain current ($\delta I^2/\delta pH^2$) as a signal response from ISFET for Carboxyl-immobilized AAs (A, R, C, D).

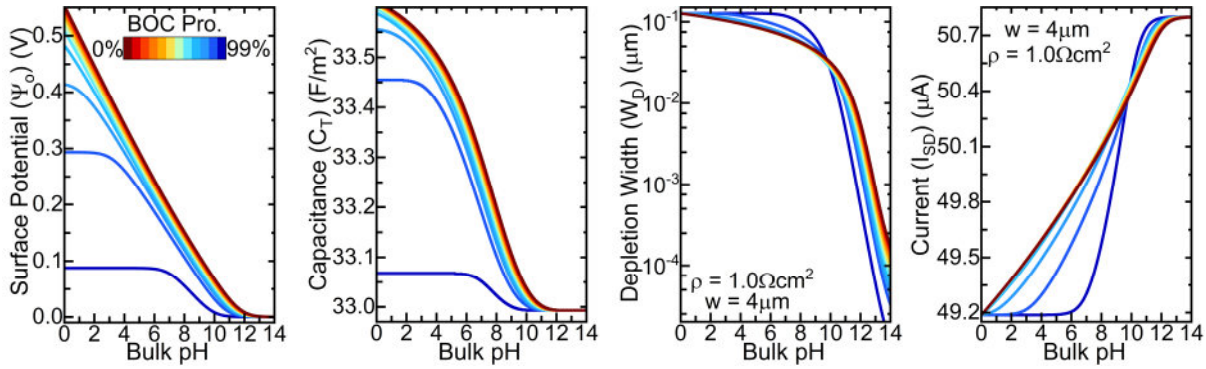

Fig. 3. Simulated characteristics for FET sensors with respect to Bulk pH (a) Ψ_o (b) C_T (c) W_D (d) I_{SD} variation for the deposited APTES in the presence of different percentages of BOC protection

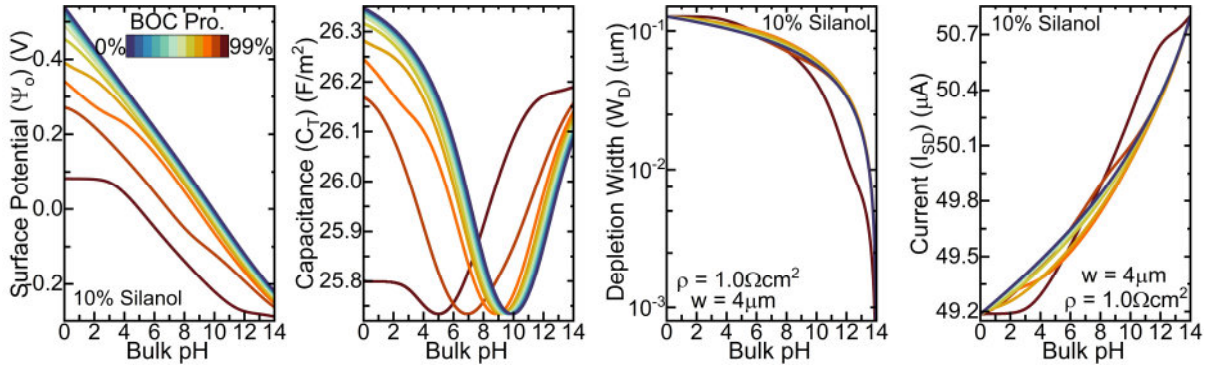

Fig. 4. Simulated characteristics for FET sensors with respect to Bulk pH (a) Ψ_o (b) C_T (c) W_D (d) I_{SD} variation for the deposited APTES in the presence of different percentages of BOC protection and 10% Silanol sites

A Data Efficient Framework for Higher Dimensional Neural Compact Modeling

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***Abstract*—This work proposes a novel framework that uses artificial neural networks (ANNs) to produce a MOSFET compact model capable of handling various device parameters, especially when the amount of data is limited. Our approach combines established knowledge transfer methods with modified meta-learning techniques, and is tested to generate current-voltage characteristics using combinations of design parameters (*e.g.* channel width, channel length, temperature). Deep ensemble techniques are also employed to estimate the uncertainty of the model predictions and to enhance their stability. The proposed framework shows excellent test accuracy, and is validated through inverter simulations. Overall, it paves a way to develop a highly accurate neural compact model for integrated circuits which can be useful for advanced devices with limited data.**

***Index Terms*—Artificial neural network, compact modeling, knowledge transfer, meta learning, ensemble, MOSFET.**

I. Introduction

As technology advances, developing analytical compact models that accurately address complex physical phenomena becomes increasingly challenging. Thus, neural compact models using artificial neural networks (ANNs) have been explored to facilitate model generation, but limited data availability can constrain their performances. To tackle this issue, a methodology was introduced in [1] that learns the physical knowledge from a well-characterized technology node, enabling accurate modeling of current-voltage (I-V) characteristics for a target device with limited data. However, the I-V model obtained through this approach cannot fully reflect the impact of device parameters, limiting its applicability in circuit simulations.

In this paper, we aim to provide a novel framework which generalizes the above approach with increased input features to model the effects of device parameters on I-V characteristics. In that regard, we develop an effective method to incorporate design parameters such as channel width (W), channel length (L), and temperature (T) and utilize the generated ANN for inverter simulations. We note that the proposed framework can be extended to include other device parameters.

II. Methodology

In this section, we extend the methodology in [1] to include the design parameters W, L, T under a data environment similar to one used for extracting parameters in analytical compact models. Specifically, we assume that only a *limited* number of I-V sweeps for a *restricted* range of W, L, T combinations (W/L/T) are measured for a target device.

The proposed modeling framework is composed of two main parts as summarized in Fig. 1. First, we apply knowledge transfer methods in [1] to generate abundant synthetic data for selected W/L/T of the target device where only few data are available. In particular, we apply meta-learning techniques [1], [2] for ANNs to learn the physics from the data of previously well-established planar MOSFET, or a *source* device, then fine-tune the ANNs on the limited target device data.

Second, we train an ANN using such synthetic data to produce abundant data for *all* W/L/T of the target device. Note that using synthetic data in training leads to uncertainty in predictions due to variations in the results produced by different ANNs from the previous step. To address that issue, we adapt the MetaFun techniques [2] to estimate such uncer-

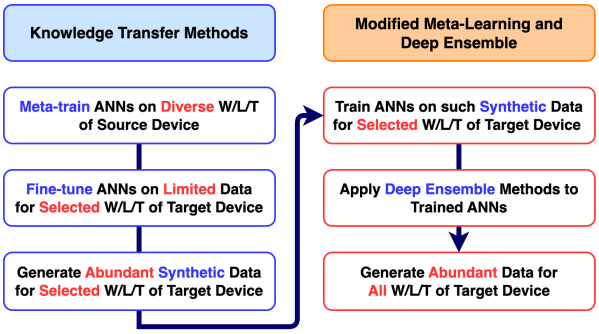

Fig. 1. Proposed modeling framework integrating previously studied knowledge transfer methods (outlined in blue) and a newly developed modified meta-learning techniques (outlined in red), aiming to generate abundant I-V characteristics for all W/L/T of a target device, despite limited availability of I-V data for a restricted number of W/L/T combinations.

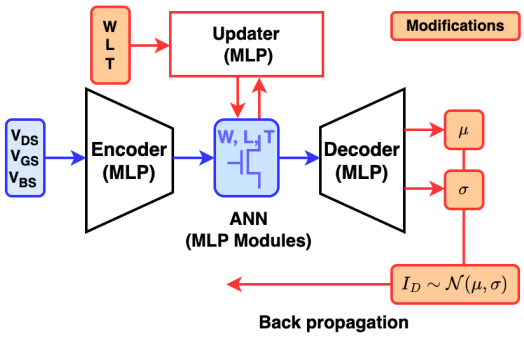

Fig. 2. Illustration of our ANN, composed of three multilayer perceptrons (MLPs) such as the encoder, updater, and decoder. The encoder and updater extract the condensed information (transistor symbol) from each W/L/T datasets directly based on the values of W, L, T and V_{DS}, V_{GS}, V_{BS}. Assisted by that information, the decoder predicts the mean μ and the standard deviation σ of a normal distribution $\mathcal{N}$ that approximates the probability distribution of I_D for the given inputs.

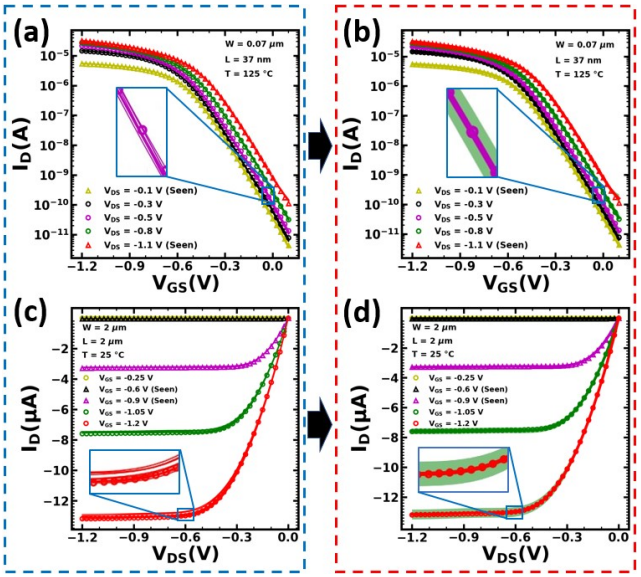

Fig. 3. I_D-V_{GS} and I_D-V_{DS} ANN predictions (lines), available data (triangles), and test data (circles) of 10 meta-trained ANNs [(a) and (c), respectively], showing that each meta-trained ANN produces slightly different predictions. Predictions (lines) of the ANN trained by our framework [(b) and (d), respectively] provide more stable fitting, along with uncertainty quantification shown as a shaded region.

tainty in addition to model the impact of W/L/T variations on I-V characteristics, as described in Fig. 2 with modifications outlined in red. Additionally, we incorporate deep ensemble methods [3]. Several ANNs in Fig. 2 are trained in parallel to maximize the probability of current I_D, and their predictions are aggregated to approximate the total predictive uncertainty.

III. Experiments

To validate our proposed framework, we utilize 45 nm N- and P-type MOSFETs as source devices, and 32 nm N- and P-type MOSFETs as target devices with the data produced by SPICE simulations [4]. For target devices, we assume that 24 I-V sweeps for each of 99 W/L/T are available, for T= $25, 75, 125$°C.

In Fig. 3, (a) and (c) show that there are variations between the synthetic data generated by each meta-trained ANN, and (b) and (d) demonstrate that the ANN implemented by our framework provides quantification of such data uncertainty, while accurately fitting the test data.

We also compare our framework with a baseline that trains randomly initialized multilayer perceptrons (MLPs) using available data for selected W/L/T of the target device, to generate synthetic data for training a final MLP.

Table I shows computational costs and test errors of ANNs trained by both methods. In our framework, 240 W/L/T with abundant data of the source device are used for meta-training [1]. For adaptation to the target device, 99 W/L/T with limited data are used. All ANNs are tested on 651 *unseen* W/L/T with abundant data. The ANNs trained by our framework show distinctively lower average test errors. Fig. 4 also shows that our framework demonstrates better accuracy and stability in predicting electrical parameters such as V_{TSAT}, V_{TLIN}, and V_{TEXT} for the same test datasets.

TABLE I
ANN TRAINED BY OUR FRAMEWORK VS. RANDOMLY INITIALIZED ANN

		Our Framework	Random Initialization
Meta-training Time		17 hours	N/A
Adaptation/Fine-tuning Time (per W/L/T)		**77.23** sec.	179.24 sec.
Training Time with Synthetic Data		7.22 hours	**3.25** hours
Relative Linear Error (%)	NMOS	**1.86**	9.48
	PMOS	**4.60**	6.59
	Average	**3.23**	8.04
Relative Log Error (%)	NMOS	**0.097**	0.36
	PMOS	**0.24**	0.33
	Average	**0.17**	0.35

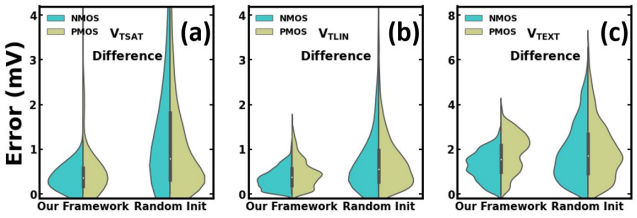

Fig. 4. Comparison of (a) V_{TSAT}, (b) V_{TLIN}, and (c) V_{TEXT} differences by ANN predictions for two methods, showing that our framework results in more stable and accurate model predictions.

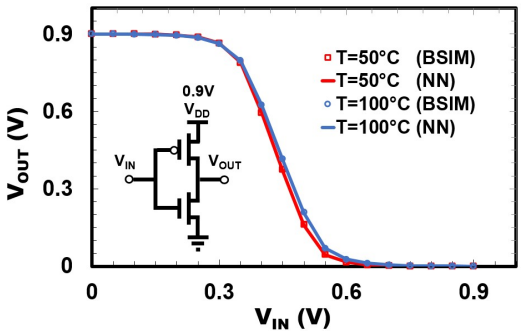

Fig. 5. Inverter simulation results by the neural compact models implemented by our framework (lines) and by BSIM4 compact models (circles) respectively, for T= $50, 100$°C, showing that the neural compact models accurately predict the operating characteristics in circuit simulations.

Finally, Fig. 5 shows highly accurate inverter simulation results by NMOS and PMOS neural compact models implemented by our framework, for unseen W/L/T.

IV. Conclusion

We generalize the neural compact modeling framework in [1] to accurately model the impact of device parameters on I-V characteristics for a target device with limited data available. Our framework produces highly accurate neural compact models for inverter simulation, and is able to estimate uncertainty to ensure the reliability of model predictions.

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Drain Bias Influence on Junctionless Nanowire Transistors Effective Channel Length

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Abstract— This paper analyzes the effective channel length (L_{EFF}) of Junctionless nanowire transistors (JNT) through the gate capacitance (C_{GG}) of the devices, for different drain-to-source voltages (V_{DS}). In this case, there is a phenomenon of intersection through the C_{GG} curves for high V_{DS} bias (between 0.5V and 1V) that indicates the pinch-off regime of the JNTs. The L_{EFF} extraction has been done from the extrapolation of the gate capacitance in the pinch-off regime as a function of the device's channel length (L_{MASK}), for different L_{MASK} and source and drain lengths (L_{SD}) for structures with lateral spacer and different doping concentrations, showing that L_{EEF} reaches ~6nm and presents a relationship with V_{DS} bias and doping concentration.

Keywords – Junctionless Transistor, Effective Channel Length, Gate Capacitance, Pinch-off.

I. Introduction

The junctionless nanowire transistor implemented in Silicon-on-Insulator (SOI) technology is a highly promising structure because it provides a significant improvement on short channel effects (SCEs), simplifies the manufacturing process because of the absence of the variation in the dopants type in the source and drain regions, and promotes a high improvement in integration scale [1-4].

This device works similarly as an accumulation mode transistor. In the case of an n-type JNT, when it is biased below the threshold voltage at the gate, no significant current flows between the drain and source since the channel of the structure is fully depleted [5]. When the gate voltage increases, exceeding the threshold voltage, the depletion region decreases, forming a body current component (I_b). When the gate voltage reaches the flatband one (V_{FB}), a new current component (I_{acc}) appears due to the current that flows by the accumulation layer [6]. The increase of the JNTs channel length overcoming the L_{MASK} in structures that feature lateral spacers has been presented in the literature [7-9], and the gate capacitance has been shown to be a good way to extract this characteristic when the structure is in the accumulation regime [8]. Thus, the aim of this work is to verify if the extraction method presented in [8], based on the gate capacitance analyses, can be applied to extract the L_{EFF} when the devices are in the partial depletion regime, specifically in the pinch-off condition, where lateral depletion influence can be observed.

II. Simulated Device and Analysis

The JNT used in this approach is similar to the presented in [7-9], and the simulated structures are the same as used in [8] with L_{MASK} varying from 30 to 100 nm, L_{SD} varying from 5 to 30 nm with doping concentrations of 5 x 10^{18} cm^{-3} and 1 x 10^{19} cm^{-3} in the channel region and spacers over entire source and drain regions. The simulations were performed using Synopsys Sentaurus 3D numerical simulator [10], and the data was validated in [8] using the JNTs provided by CEA-LETI [11].

The behavior of the gate capacitance curve, when the drain is biased, is presented in Fig. 1, and the C_{GG} as a function of V_{GS} is presented in Figs. 2-3 for V_{DS} = 0.5 and 1.0 V and different doping concentrations (N_D), respectively. In this case, one can see the intersection of C_{GG} curves when L_{SD} varies. This point indicates the V_{GS} value that conducts the structure to the pinch-off regime, which is confirmed by the analyses presented in Fig.4. Since this interception point indicates that C_{GG} is not affected by parasitic effects as source/drain lengths, L_{EFF} can be extracted by the gate capacitance in this condition. Similarly as [8], the gate capacitance is plotted as a function of L_{MASK}, which is fitted to a straight line that, when extrapolated to the zero-capacitance value, promotes a negative value of L_{MASK}. This is presented in Fig. 5, which exhibits the variation of channel length (ΔL) of the devices.

III. Conclusion

It could be observed that L_{EFF} increases for V_{DS} biases of 0.5 and 1.0 V when JNT is in the partial depletion regime and presents a dependence on both V_{DS} and doping concentration. The L_{EFF} value is around 4 to 6 nm, and the V_{DS} influence is more noticeable for lower N_D.

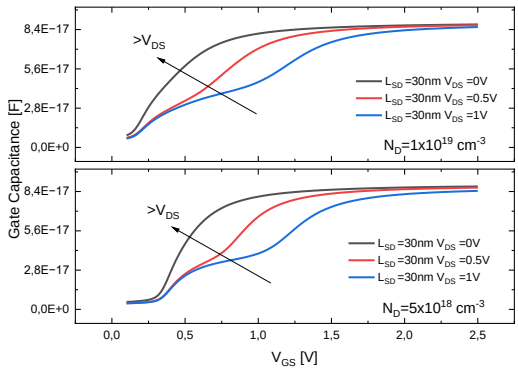

Fig.1: V_{DS} influence in Gate Capacitance as a function of V_{GS} curve.

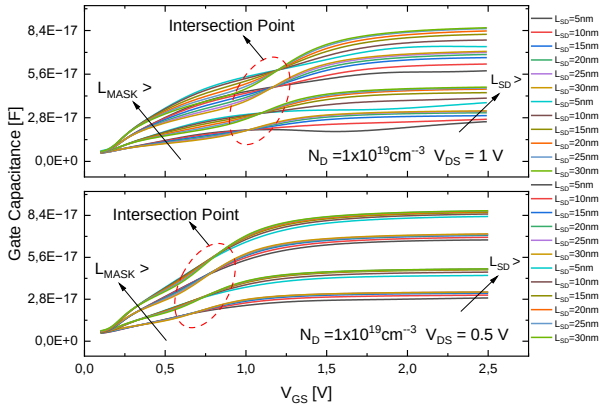

Fig.2. Gate capacitance as a function of V_{GS} for ND of $1x10^{19}cm^{-3}$and both V_{DS}.

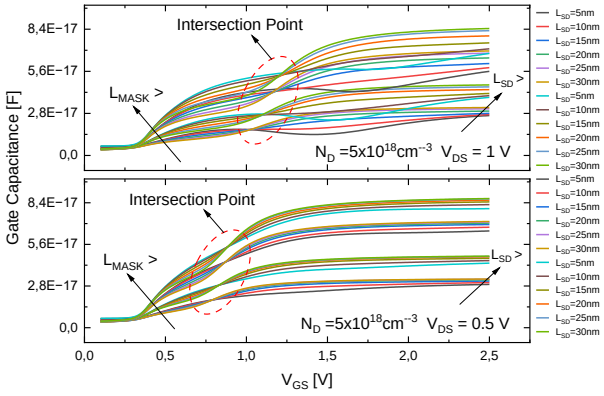

Fig.3. Gate capacitance as a function of V_{GS} for ND of $5x10^{18}cm^{-3}$and both V_{DS}

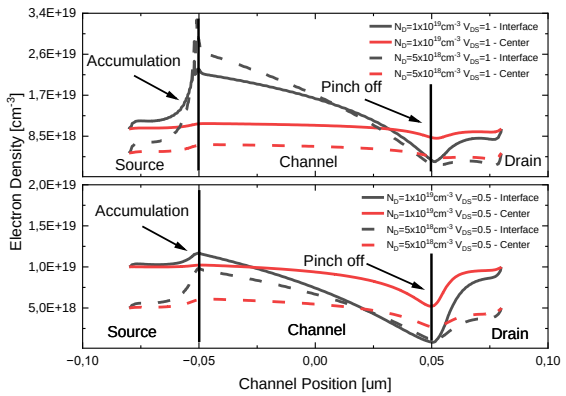

Fig.4. Electron density as a function of channel position.

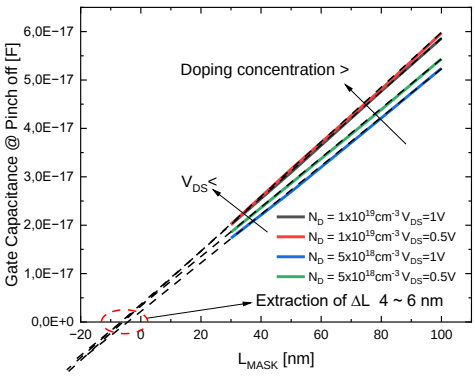

Fig. 5: Gate Capacitance (@pinch_off) as a function of L_{MASK}.

Doping concentration [cm^{-3}]	V_{DS} [V]	ΔL [nm]
1 x 10^{19}	0.5	6.51
	1	6.31
5 x 10^{18}	0.5	6.22
	1	4.1

Table 1. ΔL for different doping concentrations and V_{DS} bias.

Acknowledgments

The authors thank financial support from FAPESP, CNPq and CAPES.

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Magnetic Spin Hall induced Field-Free Magnetization Switching in SOT-MRAM Devices

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Spin-orbit torque magnetoresistive random access memory (SOT-MRAM) has been established as a promising non-volatile memory technology, offering high switching speed, low power consumption, and long endurance, due to the separation of the read and write paths.

SOT-MRAM devices take advantage of the current induced SOTs in the HM layer (Fig 1a.) mainly generated through the spin Hall effect (SHE) [1], however, to achieve deterministic switching of magnetic layers with an initial perpendicular magnetization, an external magnetic field applied along the direction of the charge current is necessary (Fig 3a). The magnetic spin Hall effect (MSHE) in antiferromagnetic (AFM) materials [2] can be utilized to overcome this limitation and to achieve field-free SOT switching. This different type of SHE results in an anti-damping-like torque, that acts to switch the magnetization out-of-plane. The switching of a perpendicularly magnetized FM layer adjacent to a MSHE-layer hast been observed in multilayer structures with a non-collinear AFM Mn_3Sn [3] layer as source of these unconventional spin currents. Spin currents and torques generated by the MSHE in an AFM/FM bilayer are depicted in Figure 2 .

We employ a fully three-dimensional finite element method (FEM) based simulation approach [4], which couples the charge and spin currents with the magnetization dynamics, to evaluate the physical phenomena responsible for the magnetization switching of SOT-MRAM devices. We model the magnetization dynamics with the Landau-Lifshitz-Gilbert (LLG) equation. A complete description of the spin torques is obtained from the non-equilibrium spin accumulation. To describe the distribution of the spin accumulation we use a coupled spin and charge drift-diffusion (DD) formalism. SOTs are included by considering the spin-charge angle tensor (SCA) reported for Mn_3Sn antiferromagnets. The SCA describes the charge-to-spin conversion and generation of additional out-of-plane spin-polarized spin currents, which lead to anti-damping like torque in the FL of the device, that is able to push the magnetizaiton out-of-plane, without the support of an external field.

In conclusion, we explore the potential of the incorporation of non-collinear AFM materials, which demonstrates the generation of non-vanishing spin-polarized current via MSHE, into SOT-MRAM devices (Fig 1b), facilitating true field-free switching in SOT-MRAM devices (Fig 3b).

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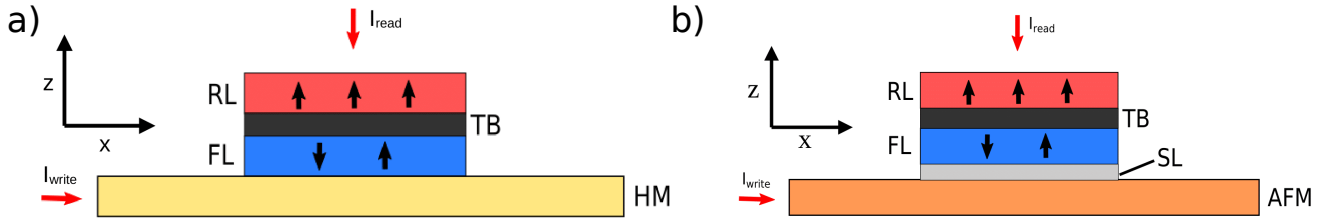

Figure 1: Schematic view of SOT-MRAM cells consisting of a ferromagnetic free (FL) and a reference layer (RL), separated by a tunneling barrier (TB), sitting on top of (a) a heavy metal (HM) layer employing the spin Hall effect (SHE) and (b) an antiferromagnetic (AFM) layer employing the magnetic spin Hall effect (MSHE). The AFM layer is separated by the FL by a Cu spacer layer for magnetic decoupling to ensure the field-free magnetization switching driven solely by the spin currents generated by the MSHE. A write current is applied along the x-direction in the HM/AFM layers. The magnetization of the FL and RL is indicated by black arrows.

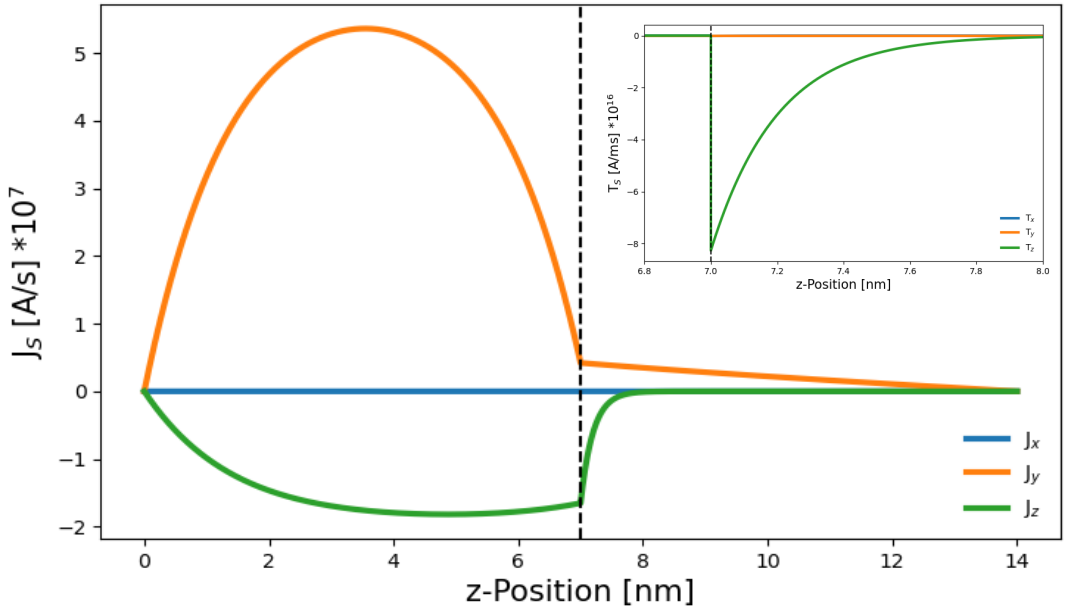

Figure 2: The spin current $\mathbf{J_s}$ and the torque $\mathbf{T_s}$ along the z-direction for a Mn_3Sn/NiCo (AFM/FM) bilayer with the MSHE. The magnetization of the FM is in-plane. A charge current is applied along the negative x-direction. Anti-damping like torques acting to push the magnetization out-of-plane are produced by the MSHE.

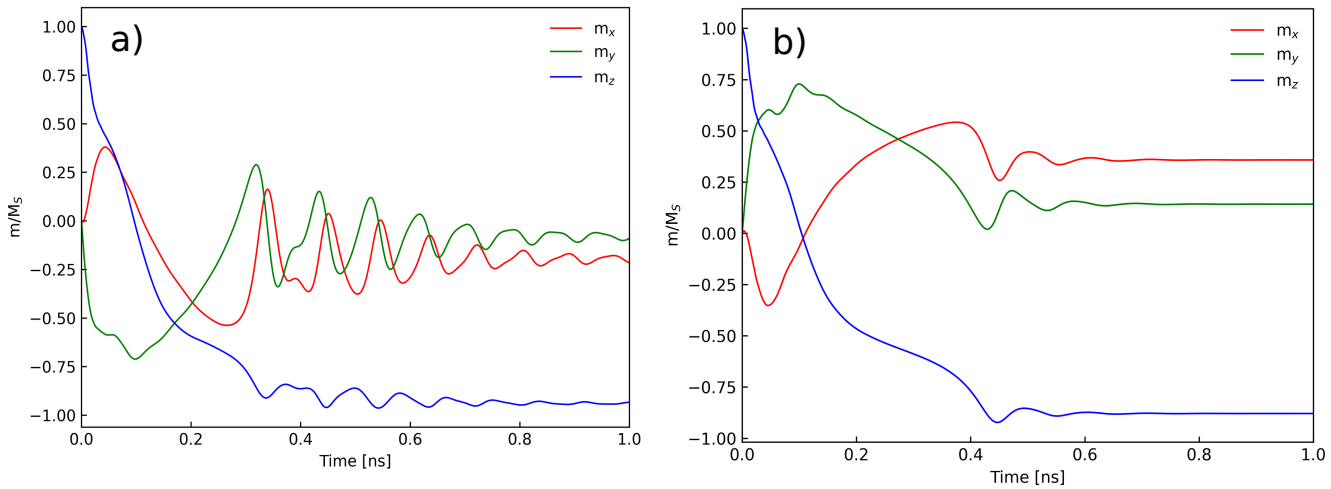

Figure 3: Perpendicular switching of an SOT-MRAM cell from a parallel to an anti-parallel state with an applied current density of 1.7 * 10^{13} A/m² (a) utilizing the SHE present in an HM layer and an additional applied external field of 0.06 T (Fig. 1a) and (b) field-free switching utilizing the MSHE in an AFM layer (Fig 1b). Due to higher spin-dephasing length in device from (b) the m_x component remains finite, as long as an SOT-current is applied. After the current is turned off m_x will relax to zero.

Novel V_{T1} Reduction Strategies in GGNMOS for Robust ESD Applications

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Electrostatic discharge (ESD) is a significant reliability concern in the semiconductor industry, leading to a wide range of IC failures. Protection circuits like gate-grounded NMOS (GGNMOS) (Fig. 1) are used to safeguard the internal circuits of an IC against ESD damage. Although studies mainly focus on enhancing GGNMOS's I_{T2} for better ESD discharge capabilities [1], downscaled devices are more susceptible to ESD damage due to the low breakdown voltages of their thin gate oxides. Most existing triggering voltage (V_{T1}) reduction techniques often complicate the GGNMOS's operation, cause gate-overdriven effects, consume on-chip area, and increase fabrication costs due to the use of ESD implants, additional mask layers, and process steps [2-6]. This article proposes novel modifications to the conventional GGNMOS structure (C-GGNMOS) to lower its V_{T1} while maintaining its current discharge capabilities (I_{T2}). This is achieved by (a) enhancing substrate hole current by a dummy gate (DG) and (b) lowering the emitter-base junction's barrier height for the parasitic lateral NPN (PL-NPN) transistor. The proposed strategies are validated through 2D TCAD TLP simulations of device structures based on a 45nm CMOS process.

Based on (a), the dummy gate-assisted GGNMOS structure (DG-GGNMOS) is proposed (Fig. 2a). During ESD events, the high potential across the DG 'pushes' a significant number of holes into the substrate (creating I_{DG}), aiding the avalanche breakdown-generated hole current (I_{AV}) in triggering the GGNMOS. To ensure DG's reliability and prevent oxide breakdown, it is constructed with a thin STI strip placed near the drain region, and its contact terminal is set as an N+ diffusion region enclosed by an n-well (Fig. 2b). In Fig. 6 and 9 the TCAD model and IV characteristics of DG-GGNMOS are shown, demonstrating a 9.19% reduction in V_{T1} compared to C-GGNMOS. In Fig. 10, DG-GGNMOS exhibits a higher body current than C-GGNMOS during triggering, suggesting the presence of an additional current source, as discussed above.

Based on (b), the barrier-lowered GGNMOS structure (BL-GGNMOS) is proposed (Fig. 3). As the doping levels of a p-n junction influence its barrier height, higher doping levels in the source region increase the barrier height ($qV_{bi,S}$), thus increasing the cut-in voltage of the source-substrate junction. This leads to an increase in PL-NPN's turn-on voltage (V_{BE}), thereby increasing GGNMOS's V_{T1}. Thus, one way to reduce V_{T1} is by lowering the doping in the source and substrate regions. Doping reduction in the substrate has its complications, but source doping reduction can be achieved by enclosing the N+ diffusion region (of the source) in an n-well. This leads to lowering of the barrier height $qV_{bi,S}$ (Fig. 3), thereby reducing V_{BE} of the LP-NPN, and thus lowering GGNMOS's V_{T1}. In Fig. 7 and 9, the TCAD model and IV characteristics of BL-GGNMOS are shown, demonstrating a 39.66% reduction in V_{T1} compared to C-GGNMOS. The slight increase in V_{hold} can be attributed to the increased resistance in the lower doped source region.

By integrating both strategies mentioned above, a merged GGNMOS (M-GGNMOS) structure is designed (Fig. 4), which further reduces V_{T1}. In Fig. 8 and 9, the TCAD model and IV characteristics of M-GGNMOS are shown. Compared to C-GGNMOS, a 48.43% reduction in V_{T1} is achieved.

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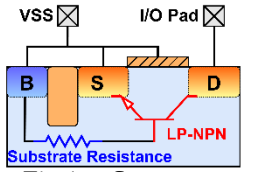


Fig 1.a: Structure

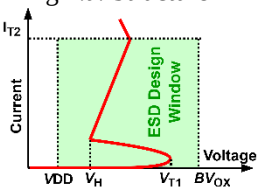


Fig 1.b: IV curve

Fig 1: C-GGNMOS

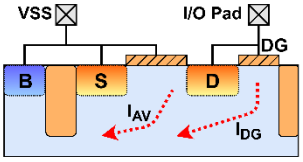


Fig 2.a: DG-GGNMOS

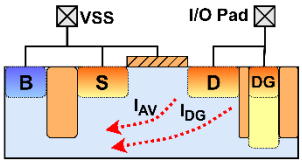


Fig 2.b: DG-GGNMOS (with STI gate)

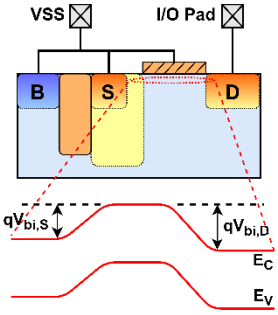


Fig 3: BL-GGNMOS

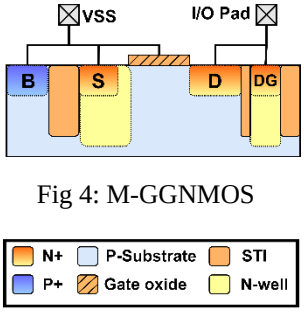


Fig 4: M-GGNMOS

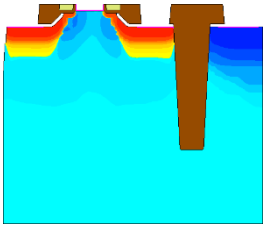


Fig 5: C-GGNMOS

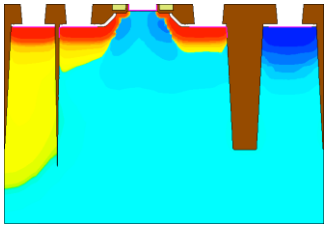


Fig 6: DG-GGNMOS

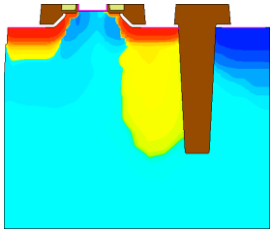


Fig 7: BL-GGNMOS

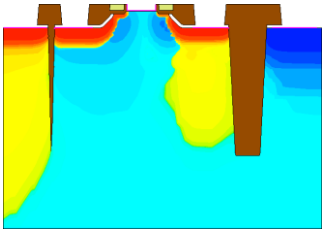
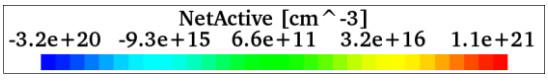


Fig 8: M-GGNMOS



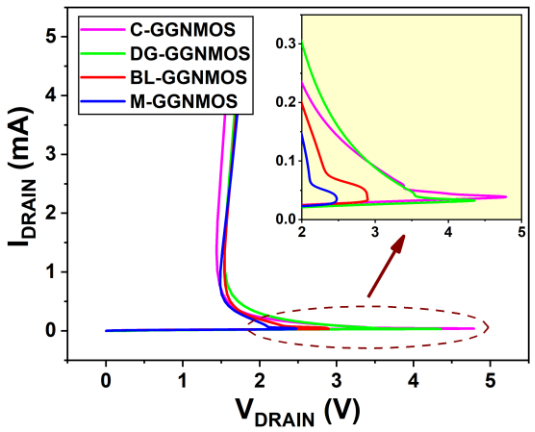


Fig 9: TCAD Simulated IV curves.

Device type	V_{T1}	% Reduction in V_{T1}
C-GGNMOS	4.79	--
DG-GGNMOS	4.35	9.19 %
BL-GGNMOS	2.89	39.66 %
M-GGNMOS	2.47	48.43%

Table 1: Table showing V_{T1} values of different GGNMOS structures.

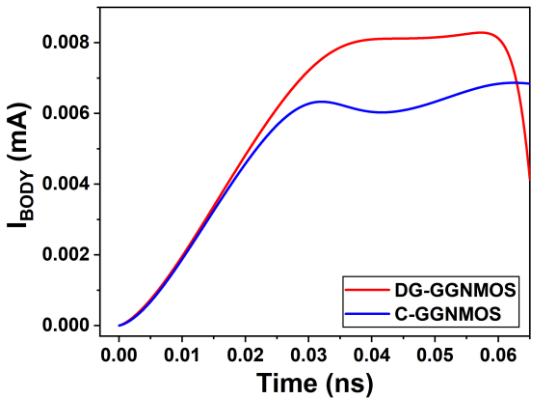


Fig 10: Body current during triggering of the GGNMOS.

Performance Investigation of 3D Stack Channel Devices

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Abstract - In this work, performance of three stacked channels iFinFET (Inserted-oxide FinFET), GAAFET (nanosheet Gate-All-Around FET) and conventional FinFET are investigated through numerical simulations. The simulated parameters such as Drain current (I_{DS}), Threshold Voltage (V_{TH}), Subthreshold Slope (SS), Drain Induced Barrier Lowering (DIBL) and Transconductance (g_m) were used as comparison tools to evaluate the performance of stacked-channel device over FinFET device. Results are demonstrating that three stacked nanosheet devices display superior DC performance indicating also better analog performance.

1. Introduction

Transistor and wire sizes are scaled to enhance speed and lower energy consumption as the electronics technology advances [1]. Bulk and SOI (Silicon on Insulator) stack channel devices are emerging as the most promising alternative for further downscaling beyond 5nm technological nodes [2, 3].

2. Simulation Setup and Results

In Figure 1, 3D simulated structures (Fig. 1a) and their cross-sectional variations (Fig. 1b, 1c, 1d) are presented. Experimental data from the literature, crucial for validating our TCAD (ATLAS from Silvaco) models and simulations [4], are depicted in Figure 2. Simulations were fine-tuned using data from Table I, along with significant parameters such as mobility, doping, models, and material specifications. For both cases, one can see good agreement between simulated and measured data.

In Figure 3, different gate overvoltage values (V_{GT} = 0.1 and 0.2 V) are used to present I_{DS} and output conductance (g_{DS}) as a function of drain voltage (V_{DS}). It can be noted that it is better in GAAFET due to the lower penetration of the drain electric field. The behavior of SS and V_{TH} is presented in Figure 4. stacked GAAFET exhibits lower V_{TH} and nearly ideal SS in devices with channel length (L) >= 16 nm; this fact occurs because these devices also exhibit better short-channel properties.

DIBL and gm are shown in Figure 5. It can be observed that as the channel length increases, DIBL is much lower in all stacked devices. From Figure 6, it is observed that the efficiency of the stacked GAAFET transistor is higher than in standard devices, mainly in weak and moderate inversion due to better SS. At low I_{DS}, SS degradation causes a decrease in g_m/I_{DS}, while the change in V_{TH} is responsible for the reduction at higher I_{DS}. When devices are operating in weak inversion, a higher value of the g_m/I_{DS} ratio can be obtained using equation (1). In strong inversion, the g_m/I_{DS} ratio reaches its lowest value and can be obtained using equation (2), where μn is the electron mobility, C_{ox} is the oxide capacitance per unit area, and n is the body factor when operating in strong inversion.

$$\frac{g_m}{I_{DS}} = \frac{ln\,10}{S} \qquad (1)$$

$$\frac{g_m}{I_{DS}} = \sqrt{\frac{2.\mu_n C_{ox}\frac{W}{L}}{n.I_{DS}}} \qquad (2)$$

3. Conclusions

The simulation results demonstrate that stacked channel structures offer greater advantages over the single channel structure with substantial replacement potential for future integrated semiconductor devices due to your better performance. For next step will be done the comparation with SOI stack channel devices.

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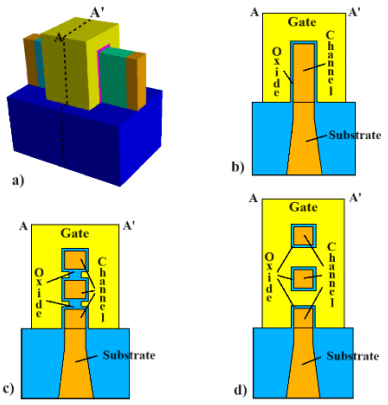

Fig. 1. Device and schematic representation of the channel cross section along the line A–A' for: a) 3D structure, b) FinFET, c) iFinFET and d) GAA FET.

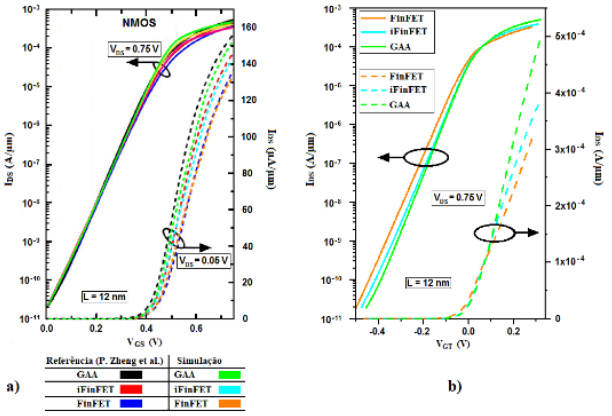

Fig. 2. In (a) Calibration of reference [4] and this work simulation and in (b) I_{DS} versus V_{GT} ($V_{GT} = V_G - V_{TH}$.)

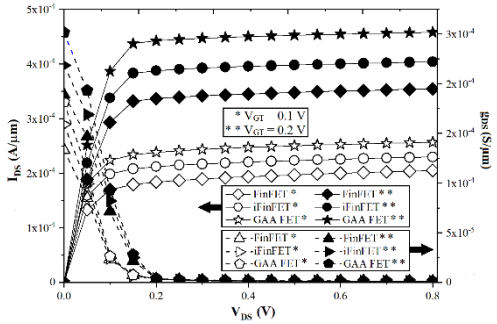

Fig. 3. I_{DS} and g_{DS} vs V_{DS} for 3D Stack Channel Devices.

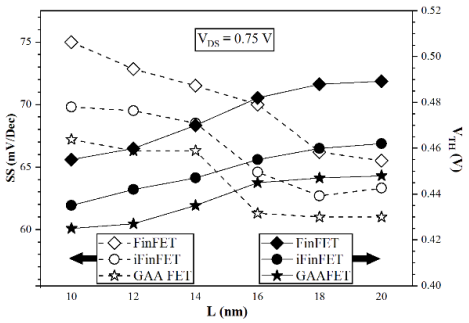

Fig. 4. SS and V_{TH} for 3D Stack Channel Devices.

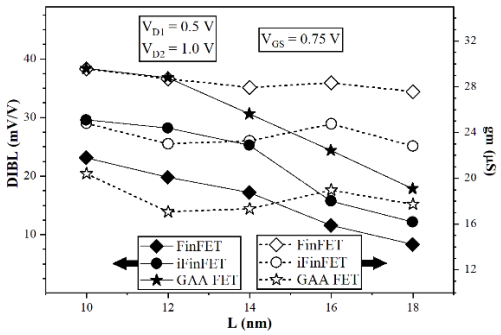

Fig. 5. DIBL and g_m for 3D Stack Channel Devices

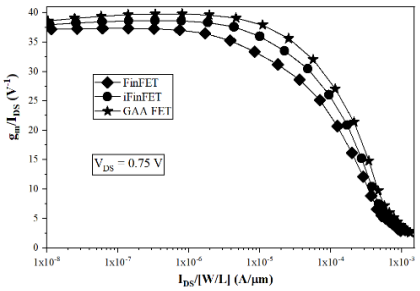

Fig. 6. Transistors Efficiency (g_m/I_{DS}) as a function of the normalized drain current ($I_{DS}/[W/L]$) for 3D Stack Channel Devices.

Table I. Transistor Design Parameter Values

Device Parameter	FinFET	iFinFET	GAA FET
W_{Fin} (nm)	6	6	6
H_{Fin} (nm)	18	6+6+6	6+6+6
L (nm)	12	12	12
Gate T_{ox} (nm)	0.7	0.7	0.7
Inserted Oxide Height (nm)	0	3.2	0
Spacing Betwenn Channels (nm)	0	3.2	6
Cross Section – W_{Fin}*H_{Fin} – (nm^2)	108	108	108

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Adaptive Body Biasing Technique based Digital LDO Regulator for Transient Response Improvement

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Digital Low-Dropout (DLDO) regulators are finding increasing usage for power management in today's ultra-low-power(ULP) systems. Specifically, as the supply levels are down-scaled to improve power efficiency, DLDOs perform better than their analog counterparts [1]. Most of these DLDOs [2-4] are based on the architecture realized in [1], as shown in Fig. 1(a). Here, the clocked comparator monitors the output voltage (V_{OUT}) and triggers the controller to change the state of the pMOSFETs in the array for V_{OUT} regulation. Since the controller turns on/off only one pMOSFET per clock cycle, there exists a trade-off b/w the size of the pMOSFET switches and the clock frequency with transient response, peak value of steady-state output voltage ripples, and power consumption of the DLDO. Fig. 1(b) illustrates the DLDO's response to a step increase in the load current (for example, a system going from sleep to active mode). Fig. 1(b) represents this event for two cases of strong/weak pMOSFETs in the array. The use of larger-sized pMOSFETs labeled as 'Strong pMOSFET' in Fig. 1(b) provides the desired shorter recovery time(T_{R1}) and reduced voltage undershoot; however, this use of strong pMOSFETs increases the peak steady-state output voltage ripples(ΔV_1). This output ripple is unavoidable due to the comparator's quantization error inherent to the DLDO's operation. We propose an adaptive body biasing technique to overcome this trade-off by dynamically tuning the pMOSFET current as described next.

In this work, we propose an Adaptive Body Biasing (ABB) technique for the pMOSFET array in the DLDO of Fig.1(a), which boosts the pMOSFETs current to load during the output voltage undershoot. The proposed method forward body biases (FBB) the body terminal of the pMOSFETs to lower their threshold voltage during the load transient periods and increase its drive current, effectively realizing the dynamic strong pMOSFETs to help meet the increased load demand. ABB circuit consists of a triggering circuit to observe the output voltage undershoot and a switching circuit for toggling the body bias of the pMOSFETs, as shown in Fig. 1(c), and the ABB circuit's operation is shown in Fig. 1(d). Since the body effect differs in SOI and bulk CMOS processes, we design and simulate the ABB-integrated DLDO in both 28nm FDSOI (RVT process) and 180nm bulk CMOS processes and report the performance improvement achieved in both the CMOS processes.

The proposed DLDO of Fig. 1(e) was designed and simulated for 0.5V reference voltage in a 28nm process (resp., 180nm); the quiescent current of the DLDO stands at 0.86µA (resp., 10.67µA) with 50 MHz F_{CLK1}. Fig. 1(f) confirms the ABB operation, where the fall of output voltage below the set threshold (V_T) toggles the body bias (V_B), and the expected boost in the pMOSFET current (I_{DS}) is observed. Referring to Fig. 1(g), for the proposed DLDO designed in 28nm CMOS process, the maximum voltage undershoot reduces from 212.3mV to 167.2mV, a 21.23% improvement and concurrently reduces the recovery time from 1.41µs to 0.83µs, a 41.13% improvement for load current change of 9.95mA over the DLDO without ABB. Fig. 1(g) also shows the increment in the current of a single pMOSFET from the array during the event of undershoot confirming the desired operation. Similarly, as shown in Fig. 1(h), for the proposed DLDO designed in a 180nm CMOS process, the reduction in undershoot voltage and recovery time for a load change of 4.95mA is 13.69% and 43.8%, respectively. Table I compares our DLDOs designed in 28nm FDSOI and 180nm bulk CMOS processes with prior DLDO works. The robustness of the design to various mismatches and process variations is justified via post-layout co-simulations, which indicates the reliable performance of the proposed DLDO in both the processes as shown in Fig. 1(i),1(j),1(k) and 1(l) respectively.

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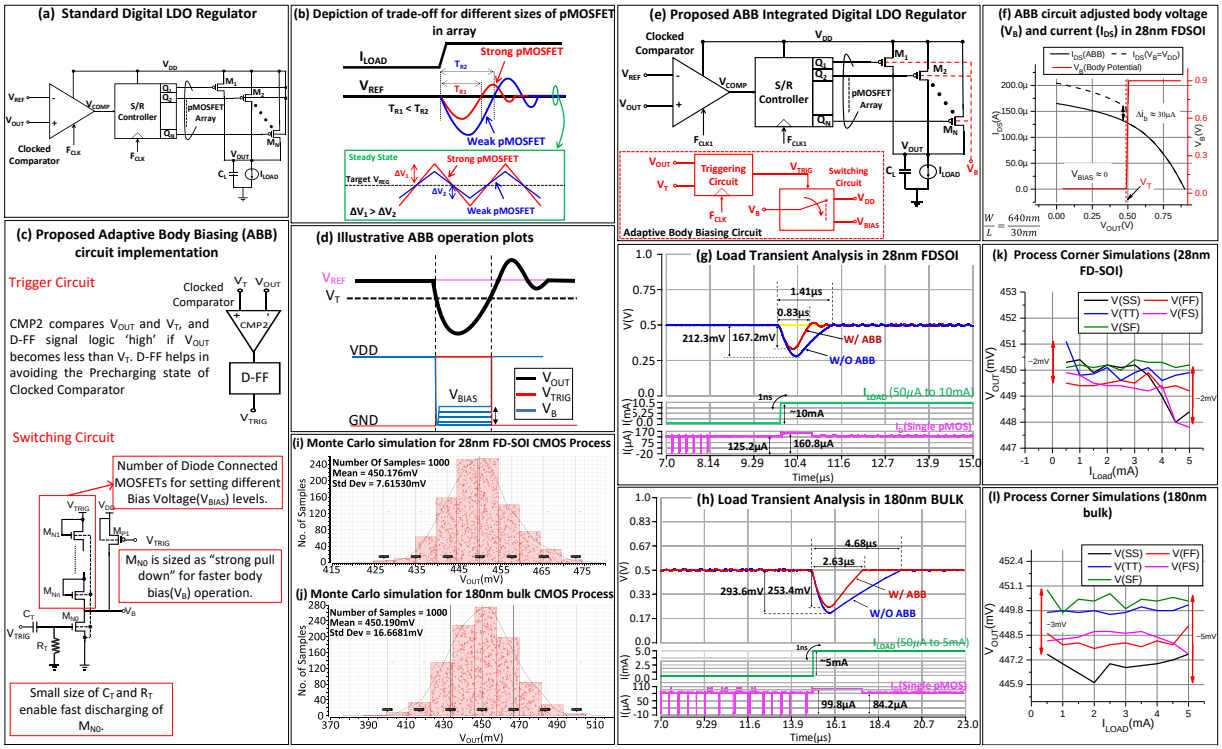

Fig. 1. (a) Standard DLDO Architecture from [1]; (b) Illustration depicting trade-offs between transient response and steady-state ripples for large/small pMOSFETs; (c) Proposed ABB circuit implementation; (d) Illustrative operation of ABB Circuit; (e) Proposed ABB integrated DLDO Architecture; (f) ABB adjusted body voltage(V_B) and current (I_{DS}) with variation in V_{OUT}; Load transient response comparison of DLDO w/ and w/o ABB technique in (g) 28nm FDSOI; (h) 180nm Bulk CMOS processes; Monte Carlo simulation of the DLDO for 1000 runs in (i) 28nm FDSOI (j) 180nm Bulk CMOS process; V_{OUT} variation in the DLDO for various process corners (SS, TT, FF, FS, and SF) with I_{LOAD} swept from 0.5 mA to 5 mA in (k) 28nm FDSOI (l) 180nm Bulk CMOS processes

Table 1 PERFORMANCE COMPARISON WITH PRIOR WORKS

Publication	[2]*	[3]	[4]*	**This Work***	
Technology	22nm FDSOI	65nm Bulk	65nm Bulk	**28nm FDSOI**	**180nm Bulk**
V_{OUT}(V)	0.5-0.7	0.55-0.95	0.5-1.1	**0.4-0.8**	**0.45-1.6**
$C_L(nF)$	0.1	1	0.5	**1**	**1**
$I_Q(\mu A)$	0.3	10.2	0.03-11	**0.86**	**10.67**
ΔI_{LOAD}(mA)	0.34	4.4	5	**9.95**	**4.95**
ΔV_{OUT}(mV)	16	118	124	**167.2**	**253.4**
$FOM_T(ps)$	4.15	62.2	27.28	**1.45**	**110.34**

$\left(FOM_T = \frac{\Delta V_{OUT} * I_Q * C_L}{(\Delta I_{LOAD})^2}\right)$; *Simulation Results

Temperature Influence on NBTI in Junctionless Nanowire Transistors

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Abstract— This paper aims to deepen the understanding of how temperature (T) influences the Negative Bias Temperature Instability (NBTI) in Junctionless Nanowire Transistors (JNTs). Thus, the study was performed through experimental measurements and simulations. It was noticed that the NBTI effect increases with T and then tends to stabilize or even decrease. This behavior differs from inversion mode device one and evidences the relative immunity of JNTs against NBTI with temperature variation.
Keywords—Junctionless nanowire transistor; NBTI; Temperature.

I. Introduction

This work deals with JNTs, which are fabricated on SOI substrates but can be distinguished from inversion mode SOI MOS transistors due to the isonomy of dopants among source, drain, and channel [1]. These regions are heavily doped with a doping concentration in the order of $1x10^{19}$ cm^{-3} [2]. The characteristics of JNTs allow them to work in partial deletion mode where the current flows mainly through the center of the channel (Fig. 1) [3]. The NBTI deleterious effect has become very important for short channel lengths [4] and is responsible for the device threshold voltage shift (ΔV_{TH}) over time [5] as shown in Fig. 2. Furthermore, this effect is due to the hydrogen used to passivate silicon/oxide interface during the fabrication process [6], which migrates away from the interface, generating interface traps [7]. These traps capture carriers from the channel, altering the V_{TH} of the device [8].

II. Experimental and Simulated Analysis

Triple gate JNTs with channel lengths (L) of 40 and 80 nm and channel width (W) of 10 and 20 nm fabricated according to [9] were measured. The transistors have a silicon layer thickness (t_{Si}) of 10 nm, an effective oxide thickness (EOT) of about 1.5 nm, and a buried oxide thickness of 145 nm. The measured devices have a p-type channel with a doping concentration (N_A) of 1 x 10^{19} cm^{-3}. For the stress process, the gate bias was kept fixed at -0.9 V for multiple cycles totaling a stress period of 10^3 s. The threshold voltage was extracted before, during, and just after the stress and the threshold voltage variation due to the NBTI (ΔV_{TH}) has been extracted at different biasing conditions, whose results are reproduced in Table 1 for the devices with L = 40 nm and W of 10 and 20 nm. Such results indicate an increase in the NBTI with the gate bias, as shown in [10]. Fig. 3 shows the ΔV_{TH} for transistors with L = 80 nm and W = 10 nm; where the black curve is the maximum amplitude of degradation during stress, and the red curve represents the V_{TH} after stress recovery time minus the initial V_{TH}. It can be observed an increase of ΔV_{TH} with T up 340 K and a reduction for higher T, which demands investigation through simulations since the results differ from the ones expected for inversion mode devices. Thus, shorter devices with L equal to 10 and 15 nm and W equal to 10 nm, which are more susceptible to NBTI, were simulated. First, the V_{TH} values without the NBTI were extracted and are shown in Fig. 4 (for L = 10 nm), and the results were used as a reference for calculating the V_{GT} ($V_{GT}=V_{GS}-V_{TH}$). Then, all devices were simulated at fixed V_{GT} values considering the NBTI degradation. V_{GT} values of -0.3 V to bias the devices into partial depletion and of -0.9 V to bias them into the accumulation regime (i.e., above the flatband voltage) were applied. In Fig. 5 (A), it is possible to observe that the ΔV_{TH} x T curves tend to stabilize and even decrease with increasing temperature for most devices. The same is repeated for the larger V_{GT} in Fig. 5 (B). In Fig. 6, it is possible to verify that with the larger $V_{GT,}$ the NBTI effect is accentuated in all cases. When the device is biased at a fixed V_{GT}, it can be farther or closer to V_{FB} depending on the temperature due to the V_{TH} dependence on T. This could result in a raise of ΔV_{TH} with T up 340 K and a reduction for higher T since the electric field of JNTs is lower at flatband condition.

IV. Conclusion

It was shown that the temperature variation certainly has an impact on the NBTI of JNTs, as it tends to stabilize or even decrease the V_{TH} shift with the increase in temperature up to 380 K.

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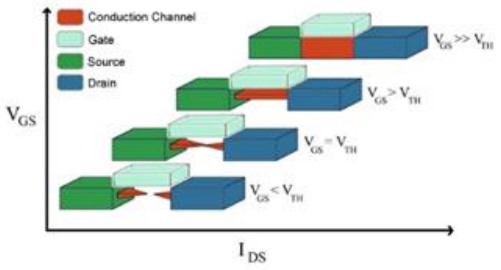

Fig.1: *Behavior of JNTs with V_{GS} increase in the formation of conduction channel.*

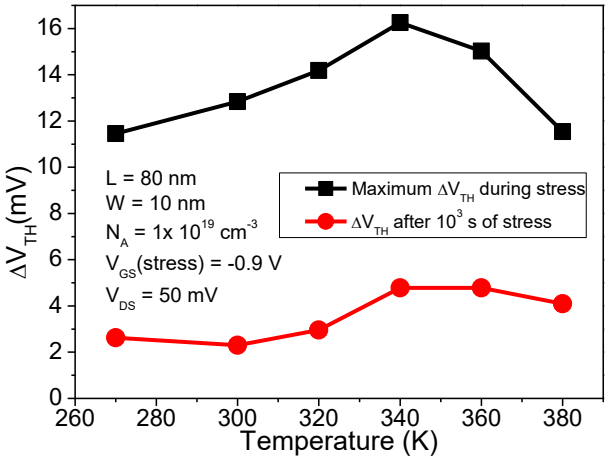

Fig.3. *Experimental ΔVTH vs. T for JNTs of L = 80 nm at V_{GS} = -0.9 V.*

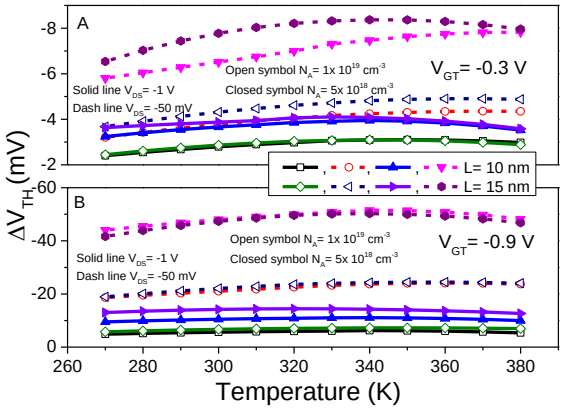

Fig.5: *Simulated ΔV_{TH} vs. T for JNTs of L = 10 and 15 nm, (A) for V_{GT} of -0.3 V and (B) for V_{GT} of -0.9 V.*

W [nm]	V_{GT} [V]	ΔV_{TH} [mV]	
		Experimental	Simulated
10	0.3	-2.8	-2.8
	0.5	-2.7	-4.0
	0.7	-4.4	-4.8
20	0.3	-3.6	-3.2
	0.5	-3.2	-3.2
	0.7	-4.4	-4.4

Table 1. *ΔV_{TH} due to NBTI in experimental and simulated devices of L = 40 nm, N_A= 1x10^{19} cm^{-3}, T = 300 K and V_{DS} = -0.05 V.*

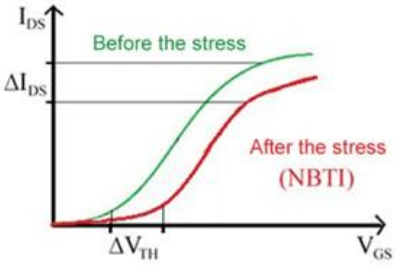

Fig.2. *Illustration of the NBTI effect on the Ids x V_{GS} curves of a FET.*

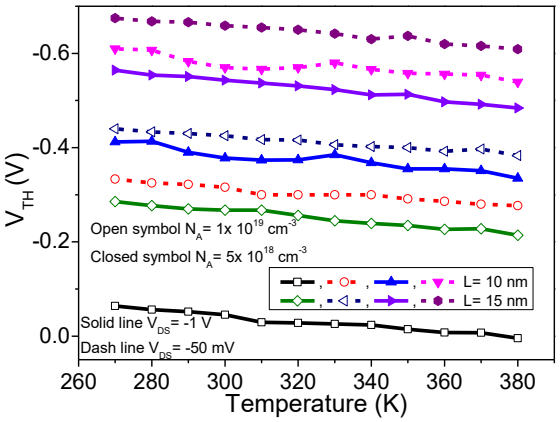

Fig. 4: *V_{TH} x Temperature curve (without NBTI) for JNTs of different L.*

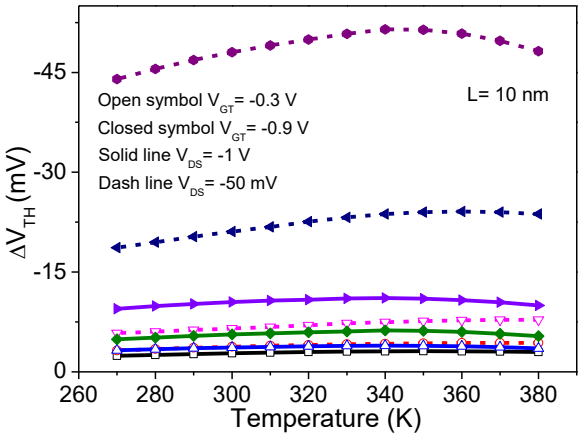

Fig.6: *Simulated ΔV_{TH} vs. T for a JNT of L = 10 nm at V_{GT} of -0.3 and -0.9 V.*

Acknowledgments

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Body Bias Assisted Method for Improvement in Performance Parameters of Analog Compute In-Memory Architecture

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Recent advancements in artificial intelligence (AI) for different applications have led to increase in demand for deep neural networks (DNN), especially in edge devices. The basic operation and computationally data intensive task in DNNs is multiply-and-accumulate (MAC). AI hardware implementation requires low power consumption, high speed, and less area where edge devices have an added constraint of limited memory storage. The limitations of conventional von-Neumann based architectures are overcome with compute in-memory (CIM) architectures. In CIM architectures, the excessive data movement between process and memory units is reduced by performing the MAC operation inside the array itself. The bit precision of weights and input being used can also be modified as per the desired accuracy of the CIM architecture. Since the data movement is reduced, therefore, significant improvements in both speed and energy efficiency are observed for CIM architectures with minimal loss in accuracy. The CIM architectures can be classified into two categories: (a) Near Memory Computing (NMC) (b) In-Array Computing (IAC) as shown in Fig. 1.

In this article, we propose a body bias (BB) assisted method for the improvement in performance parameters (number of simultaneous row activation and signal margin) of a given compute in-memory (CIM) architecture. This task is accomplished by applying appropriate bias voltage on body terminal of NMOS/PMOS devices employed in a 6T SRAM bit cell. The applied bias voltage results into improvement in the read current of the transistors which increases the bitline voltage discharge thereby allowing high throughput while achieving desired level of signal margin. The proposed method is applicable to any SRAM based analog CIM architecture. We observed that with the application of body bias, we can achieve upto 3× improvement in the performance of the CIM architectures. The simulation work is carried-out in STMicroelectronics (STM) 28 nm FDSOI process. The available body bias range on STM 28 nm process is -3 V to +3 V for RVT devices. We execute this task with the help of following steps:

1. We, first, evaluate the impact of body biasing on a single MOS device and how it controls the threshold voltage and I_{ON}/I_{OFF} ratio in a MOS device as shown in Fig. 2.
2. We use the feature of body bias to control the bitline discharge in a single SRAM cell and then extend it to multiple row activation of SRAM cells in the analog CIM architecture (Fig. 3).
3. Development of a design method for the application of body bias to improve signal margin and throughput of for any given analog CIM architecture as shown in Fig. 4 and the results are shown in Fig. 5(a).
4. Application of the proposed methodology on existing state-of-the-art CIM architecture, resulting in an improvement of 3× in the number of operations and 3.2× in signal margin (Fig. 5(b)).

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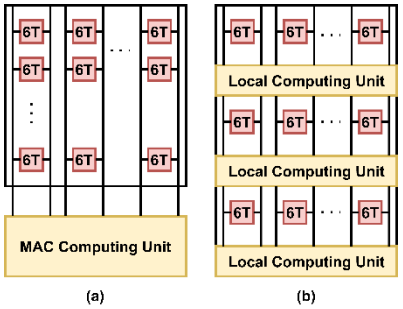


Fig. 1. Different types of analog CIM architecture (a) Near Memory Computing (NMS) (b) In-Array Computing (IAC).

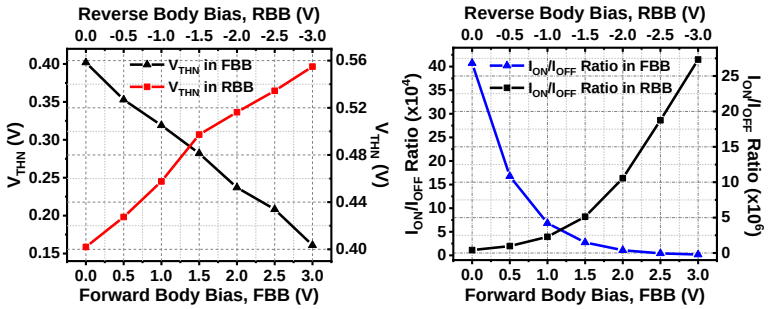


Fig. 2. (a) Variation of threshold voltage with body bias, and (b) Variation of I_{ON}/I_{OFF} ratio with body bias.

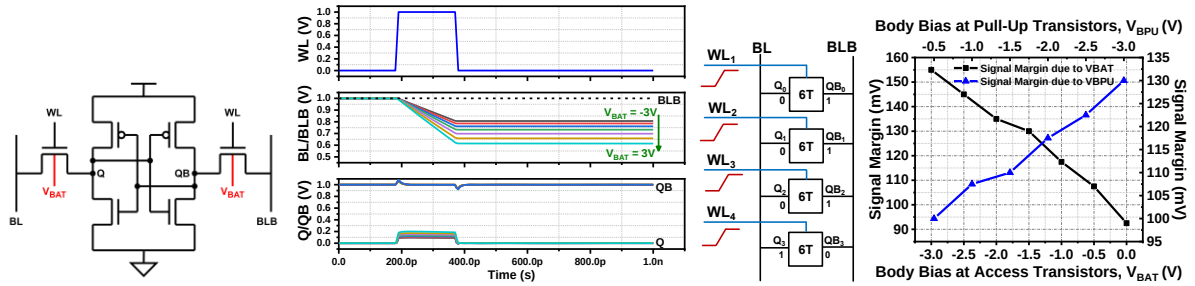


Fig. 3. (a) Schematic of a 6T SRAM Cell (b) Bitline discharging in single SRAM cell due to BB. (c) Multirow activations with 6T SRAM Cell. (d) Variation of Signal Margin with body bias at access and pull-up transistors in 6T SRAM.

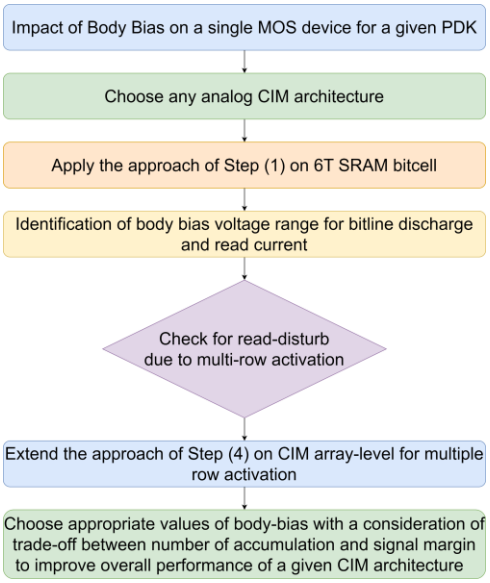
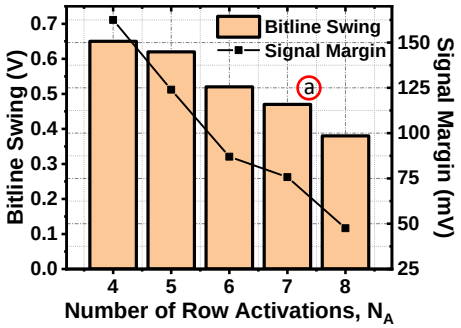


Fig. 4. Proposed design method for the application of body bias to improve signal margin and throughput in any given CIM architecture.



b

Parameters	Ref [1]	Ref [2]	Ref [3]	Ref [4]
Weight/Input Bit Precision	4/4	4/4	1/4	4/4
Without Body Bias				
Signal Margin	16.75 mV	33.5 mV	102.5 mV	21 mV
No. of Accumulations	4	4	4	4
With Body Bias				
Signal Margin	53.12 mV	65 mV	115 mV	58 mV
No. of Accumulations	12	8	4	12

Fig. 5. (a) Trade-off between number of row activations and signal margin with $V_{BAT} = -3V$ and $V_{BPU} = -3V$. (b) Comparison of CIM Array parameters for various MAC schemes with and without body bias.

Assessing the Performance of Ferroelectric Junctionless FET for NVM

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***Abstract*:** In this article, we provide physical insights into the operation of Junctionless Ferroelectric SOI (JL-FE-SOI) using preisach based FE model in technology computer aided design (TCAD). This study expands on this understanding by examining how extrinsic FE variations and underlying transistor variations impact the performance of FeFET. Our findings reveal that (1). for JL-SOI, the underlying device variations impacts the sense ratio (S.R.), I_H/I_L (PRG current/ERS current) significantly, (2). the FeFET variations can be reduced by reducing the doping concentration of the baseline JL-SOI FET and (3). at low P_R and E_C values we observed increased variability due to reduced impact on the channel electrostatics.

Introduction: The FE polarization controls the FeFET threshold voltage (V_{TH}) and the stored FE state is read out from the channel conduction. The JL-FE-SOI reduces the fabrication hurdles due to its reduced process flow [1]. However, the heavily doped channel in the JL devices introduces variability due to film thickness (T_{si}) and channel doping (N_{ch}).

Our results reveal that not only the FE parameters significantly increases the variations but the intrinsic baseline transistor parameters too have a much stronger impact. *Hence, strategies to mitigate variations should not only target the extrinsic FE parameters but also the underlying transistor parameters for JL-FE-SOI.*

Result and Discussion: The process variation dependence of the intrinsic baseline transistor (t_{si}, N_{sub}) parameters are studied. In JL-FE-SOI, the conduction is due to the formation of a conductive path whose width keeps increasing with gate bias and primarily is due to bulk conduction. Fig.1 and fig. 2 shows the motivation of the work and the simulation setup respectively. Fig. 3 shows the memory characteristics of the JL memory cell. The observed memory window and sense ratio is 1.12V and $4.2\text{x}10^4$, respectively. At first, the impact of different channel thickness on memory characteristics is observed, as shown in fig. 4(a). Then, impact of process variation (±10%) in T_{Si} is observed on MW and SR as shown in fig. 4((b)-(f)). It is observed that the $\sigma V_{TH,H}$ and $\sigma V_{TH,L}$ for JL-FE-SOI is higher in comparison to σMW (fig.4(c-d)). Further, the variation in SR is more when compared to σMW. Due to increased variation in the conduction path formed from the bottom of the channel, σI_L (erase state) varies significantly at V_{GS}=0, but the relative change in channel potential ($\psi_H - \psi_L$) is negligible for both the states. Hence, the change in MW is insignificant, but the slight change in ψ_L brings a considerable change in I_L. At low channel doping, these variations can be further reduced (fig.5). Fig.6 shows the contour plot of the electron density in the channel region for different T_{Si}. Now, consider a ±10% variation in N_{sub} as another underlying device parameter. Fig. 7(a) shows the memory characteristics of the cell with varying N_{sub}. Again, the change in MW is insignificant, but the change in SR is considerable. The change in channel surface potential with varying N_{sub} is significant for the ERS state (fig.7(b-f)). Fig.8 shows reduced process variability due to N_{sub}. Fig. 9 shows an increase in the conductive path for the ERS state as we increase N_{sub}. The conductive path starts to form from the bottom of the channel, hence a change in N_{sub} changes the drop across the depletion region formed in the channel region, reducing the FE switching activity. The combined effect of increased conduction path and reduced P_R with increasing N_{sub} increases the variability in I_L again at $V_{GS} = 0$V and impacts the SR considerably.

Conclusion: It is shown that the MW is process invariant, whereas SR shows significant variation with T_{si} and N_{sub}. At low channel doping, we have observed reduction in process induced variability. At low P_R and E_C, we have observed significant increase in process variations as compared to high P_R and E_C.

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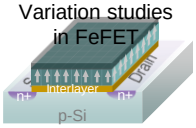
Motivation: Impact of Intrinsic Underlying Transistor Variation on the Performance of Ferroelectric Junctionless SOI FET

Previous studies

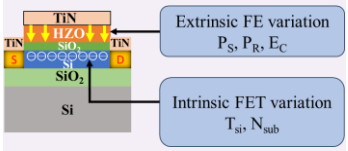
Intrinsic switching dynamics [2] (Stochasticity, domain discreteness)

Baseline transistor variation [2] (LER, RDF, WF, SR)

Variation studies in FeFET



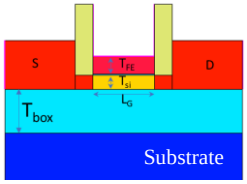
This work

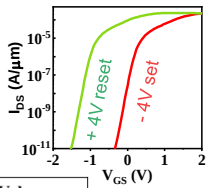


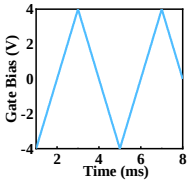
Different sources of variability in Junctionless FeFET: Extrinsic FE parameters variation, and intrinsic baseline transistor variation.

Fig.1. Reliability issues in Ferroelectric FET

Junctionless FE SOI FET







Parameter	Value	Parameter	Value
L_G	35 nm	$N_{source/drain}$	$5x10^{19}$ cm^{-3}
T_{si}	8 nm	T_{box}	25 nm
EOT	1 nm	P_S	23 μC/cm^2
T_{FE}	8 nm	P_R	21 μC/cm^2
N_{sub}	$1x10^{19}$ cm^{-3}	E_C	1.0 MV/cm

Fig.2. Schematic and device dimensions of Junctionless FE FDSOI

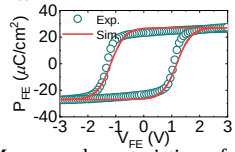


Fig.3. Memory characteristics of Junctionless FeFET with calibrated ferroelectric parameter.

Impact of Silicon Channel Thickness (T_{si}) on the Memory Window and Sense Ratio

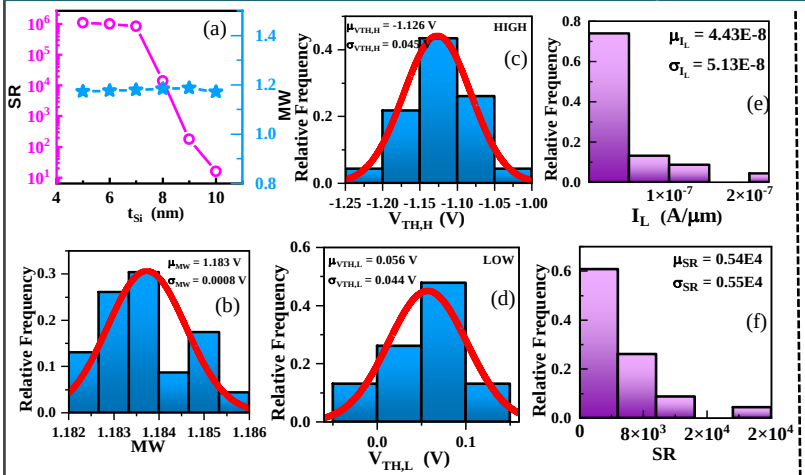


Fig.4. (a). Shows the variation in SR and MW for different t_{si} , (b). shows the impact of process variation considering only t_{si} on the MW, and (c-d). HIGH and LOW memory state, (e). shows the variation in current at V_{GS}=0 V in LOW state (I_L), (f). shows the histogram of the sense ratio.

Reduced Doping

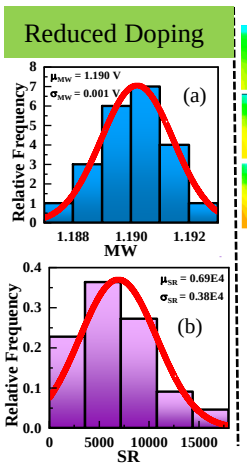


Fig.5. Shows the process variation in t_{si} on (a). MW and (b). SR for reduced channel doping. The variation in the performance has reduced due to the increase in depletion width. This can also be seen in fig. 6.

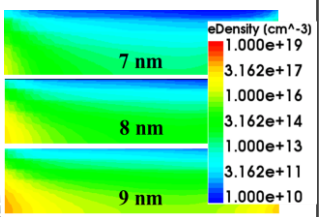


Fig.6. Shows the electron density for different channel thickness. For the case Tsi=9nm, the electron concentration at the bottom of the channel increases leading to increase in current.

Impact of channel doping (N_{sub}) on the Memory Window and Sense Ratio

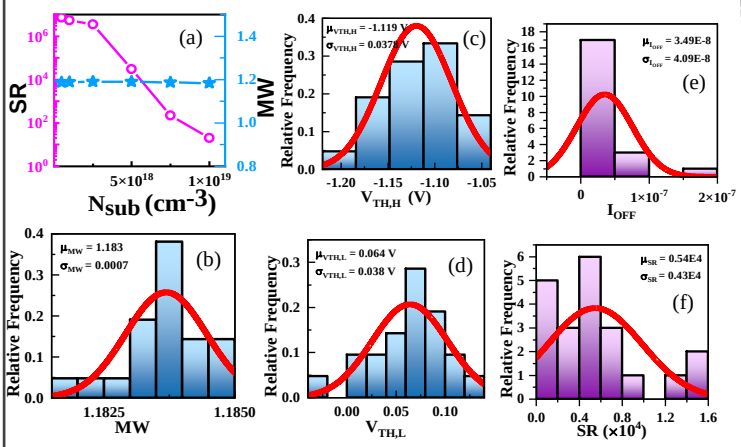


Fig.7. (a). Shows the variation in SR and MW for different N_{sub} , (b). shows the impact of process variation considering only N_{sub} on the MW, and (c-d). HIGH and LOW memory state, (e). shows the variation in current at V_{GS}=0 V in LOW state (I_L), (f). shows the histogram of the sense ratio.

Reduced Doping

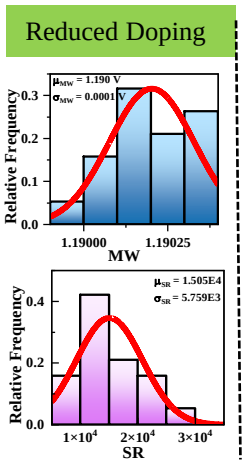


Fig.8. Shows the process variation in N_{sub} on (a). MW and (b). SR for reduced channel doping. The σMW and σSR has reduced due to the increase in channel conduction path. This can also be seen in fig. 9.

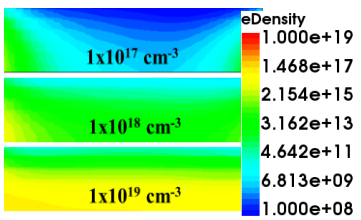


Fig.9. Shows the electron density for different channel doping concentration. For N_{sub} = 9nm, the electron concentration at the bottom of the channel increases leading to increase in conductivity.

Silicon-oxide resistive switching memory based on the HSQ layer

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Resistive Random Access Memories (RRAM) have been extensively studied due to their potential application in emerging computing paradigms [1]. Many dielectric materials have been studied as a resistive switching layer, including silicon-oxide [2], which is the most studied dielectric used in the semiconductor industry. We present the study of silicon-oxide resistance-switching memory based on the spin-on layer [3]. We used hydrogen silsesquioxane (HSQ) as a resistive switching layer in MIS (Metal-Insulator-Semiconductor). It is a silicon-oxide-like material commonly used as a resist layer in electron-beam lithography. Devices were fabricated on a highly doped n++ Si wafer. HSQ layer was spun on a wafer using a spin-coater. Layers with different thickness values were obtained by controlling the spin-coating speed. After coating, we performed annealing in 350^{O}C or 500^{O}C. Subsequently, top and bottom Al electrodes were fabricated. In Fig. 1, we present the schematic of the fabricated structures. Devices were electrically characterized using the Keithley 4200A-SCS Parameter Analyzer. We studied the properties of the fabricated devices. In Fig. 2, we present the current-voltage characteristics of an exemplary device. In Fig. 3, we show the I-V curves in a log-log scale, revealing the Space Charge Limited Conduction mechanism in the High Resistance State (HRS) and Low Resistance State (LRS). In Fig. 4, we show cumulative distribution function (CDF) of read current in HRS and LRS. In Fig. 5, we present the retention in LRS and read current values for different device areas. This work presents the study on silicon-oxide resistance-switching memory based on the HSQ layer, showing that HSQ is a promising candidate for a resistive switching layer with a simple fabrication process.

Acknowledgment

Research was funded by the Warsaw University of Technology within the Excellence Initiative: Research University (IDUB) programme.

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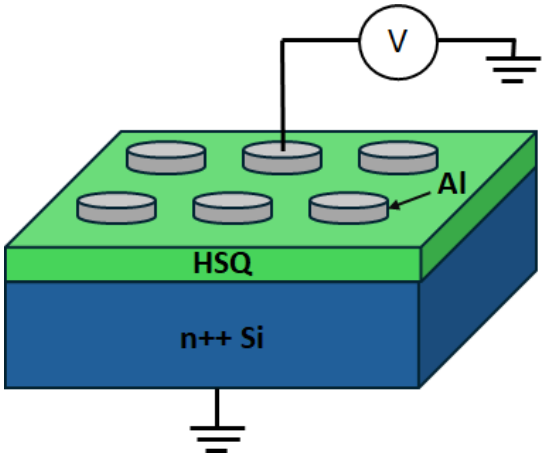

Fig. 1. Schematic structure of the fabricated RRAM devices with various electrode radius R (50 um, 100 um, 150 um).

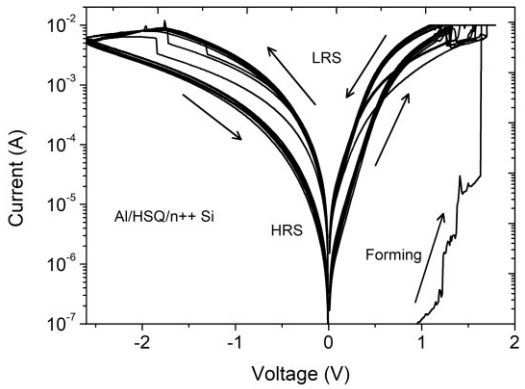

Fig. 2. Current-voltage characteristics of Al/HSQ/n++ Si RRAM device, HSQ thickness d = 35 nm, R = 100 um.

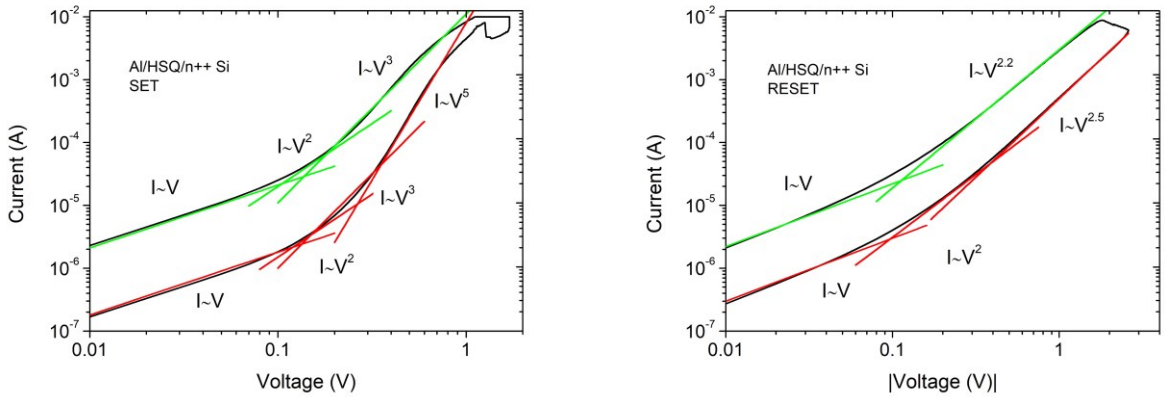

Fig. 3. Current-voltage characteristics of Al/HSQ/n++ Si RRAM device in log-log scale. SCLC transport mechanism is visible for HRS and LRS in SET and RESET cycles.

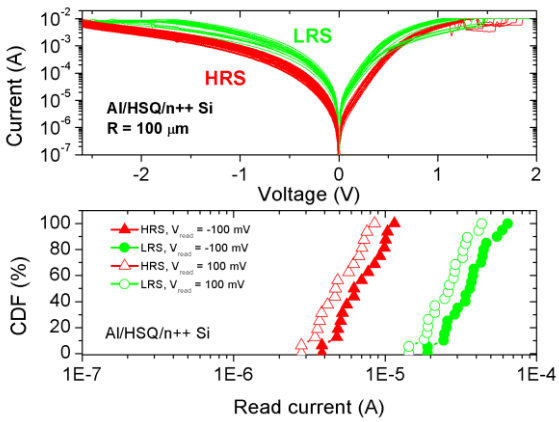

Fig. 4. I-V characteristics and CDF of read current for Al/HSQ/n++ Si RRAM device (HSQ thickness d = 35 nm, R = 100 um).

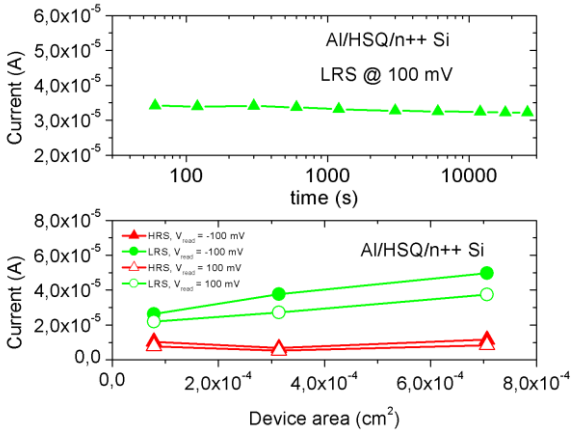

Fig. 5. Retention in LRS and read current vs electrode area for Al/HSQ/n++ Si RRAM device (HSQ thickness d = 35 nm, R = 100 um).

Study of RRAM devices with PECVD silicon-oxide resistive switching layer

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Resistive Random Access Memory (RRAM) is one of the emerging non-volatile memories intensively studied in recent years due to the potential of scaling and application in novel computing paradigms [1][2]. Silicon oxide is a well-known dielectric in semiconductor technology that can be fabricated using various techniques. In this work, we study RRAM devices with a silicon-oxide layer fabricated by PECVD (Plasma Enhanced Chemical Vapor Deposition). We fabricated a MIM (Metal-Insulator-Metal) RRAM structure using standard CMOS technologies on an oxidized silicon wafer. The bottom (Cr) and top electrodes (Al, Ni) were deposited using magnetron sputtering and patterned using UV lithography and plasma etching. SiO_x layer was deposited using PECVD. Processes with various parameters were tested to find the optimal ones for the fabricated devices regarding the device performance. Electrical characterization of fabricated devices was performed using the Keithley 4200A-SCS Parameter Analyzer. In Fig. 1, we show the schematic structure and optical microscope photo of fabricated RRAM devices. In Fig. 2, we present the current-voltage characteristics of Al/SiOx/Cr devices after multiple cycles between LRS (Low Resistance State) and HRS (High Resistance State). In Fig. 3, we show the identified transport mechanism in HRS and LRS. In HRS, for low voltage values it is Schottky emission, whereas for higher voltages we observe Poole-Frenkel transport mechanism. In LRS, we observe ohmic conduction. In Fig. 4 and Fig. 5, we present the cumulative distribution function (CDF) of SET/RESET voltages and read current in HRS and LRS, respectively.

In this work, we present the study of Al/SiOx/Cr MIM RRAM devices with silicon-oxide fabricated using PECVD. We measure and analyze the electrical characteristics, showing that devices exhibit good resistive switching properties, which makes them an interesting candidate for novel non-volatile memory.

Acknowledgment

Research was funded by the Warsaw University of Technology within the Excellence Initiative: Research University (IDUB) programme.

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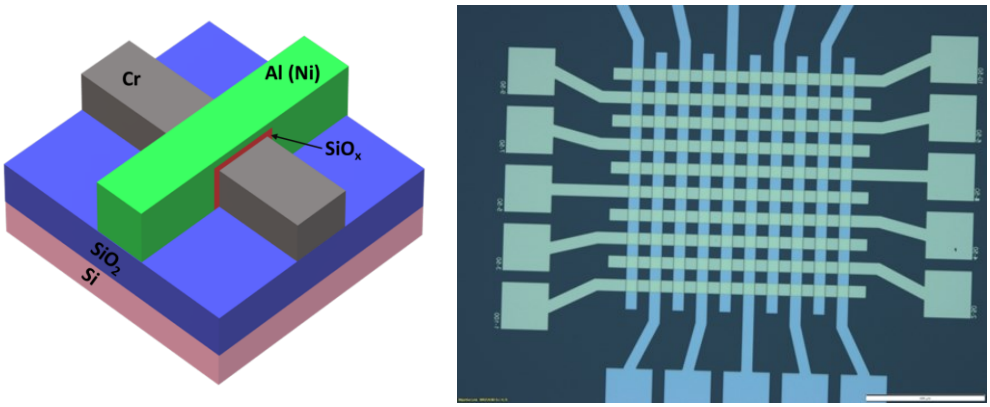

Fig. 1. Schematic structure and top-view optical microscope photo of the fabricated Al(Ni)/SiO_x/Cr RRAM devices (scale bar – 500 um).

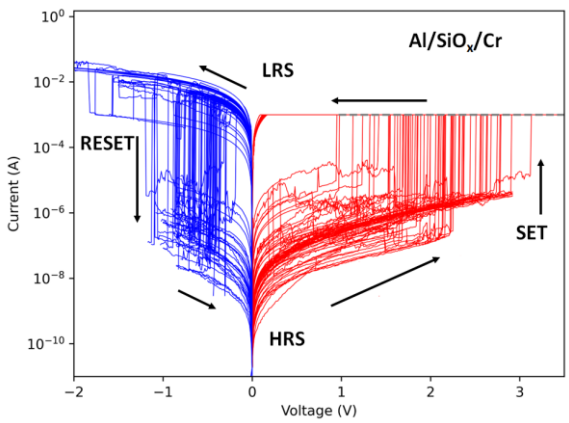

Fig. 2. Current-voltage characteristics of Al/SiO_x/Cr RRAM after multiple cycling (device area of 50x50 um^2, 60 cycles).

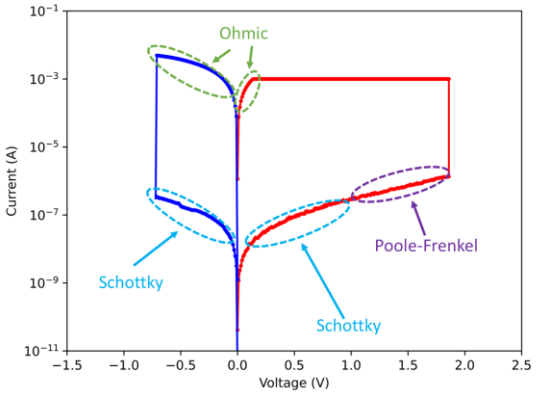

Fig. 3. Current-voltage characteristic of Al/SiO_x/Cr RRAM with indicated transport mechanisms for various voltage range (device area of 50x50 um^2).

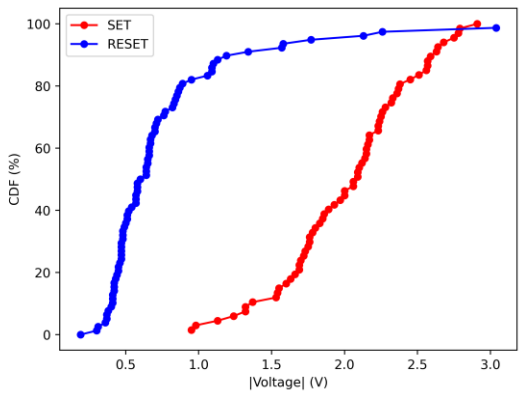

Fig. 4. Cumulative distribution function of SET/RESET voltages for Al/SiO_x/Cr RRAM (device area of 50x50 um^2, 60 cycles).

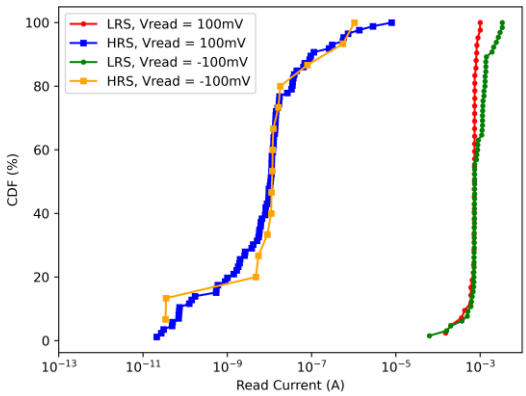

Fig. 5. Cumulative distribution function of read current for Al/SiO_x/Cr RRAM (device area of 50x50 um^2, 60 cycles).

Small Signal PDSOI MOSFET model: Considering Impact Ionization and Self Heating Effects.

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The floating body (FB) Effect in PDSOI (Partially Depleted Silicon on Insulator) MOSFETs has traditionally been viewed as a concern due to its potential to induce variations in device performance [1]. However, this phenomenon presents unique opportunities for enhancing energy efficiency, also the ability of the floating body to modulate threshold voltage facilitates improved headroom in analog circuit design, enabling enhanced performance and functionality for low-voltage applications. By highlighting the untapped potential of this well-established technology, we propose a novel FB Potential model considering impact ionization (II) and Self-Heating (SH) effects, for low terminal bias (V_{DS} and V_{GS}). Based on this, we derive a small signal model for PDSOI MOSFET. A well-calibrated Sentaurus TCAD setup is employed for the analysis of a 180nm PDSOI device using appropriate mobility, SH, and II models against the experimental data provided by SCL as shown in Fig. 1(a) & 1(b) respectively. To understand the behavior of FB and SH effect on PDSOI device, we first analyzed the impact of terminal bias on the device characteristics [2]. Fig. 2(a) depicts the FB analysis with terminal bias, which is crucial for understanding the device's characteristics. Additionally, we also explored the SH effect in PDSOI device, as illustrated in Fig. 2(b). To develop a model for FB potential while considering II and SH effects, we initially estimate an Ionization coefficient model $(\alpha_{ii} = I_{ii}/I_{DS0})$, [3] that incorporates II effects as depicted in Fig. 3(a) and 3(b) respectively for a body-tied-to-ground (BTG) PDSOI device. Fig. 4 illustrates the relationship between body-to-source current (I_{BS}) and FB potential. Following this, FB potential is deduced to be the potential where I_{ii} equals I_{BS}, as illustrated in Fig. 5(a). The proposed FB potential model is validated using a calibrated TCAD setup, as shown in Fig. 5(b). Subsequently, we have proposed an FB-dependent Ionization coefficient (α_{model}) and drain current ($I_{DS_{model}}$) model shown in Fig. 6(a) and 6(b) respectively. These models are then utilized to develop a model, for small signal parameters (g_m and R_o) for PDSOI device, with validation against the calibrated TCAD setup shown in Fig. 7(a) and 7(b) respectively.

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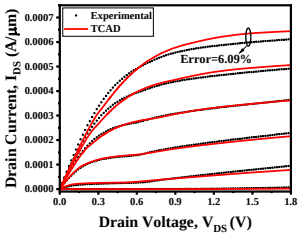


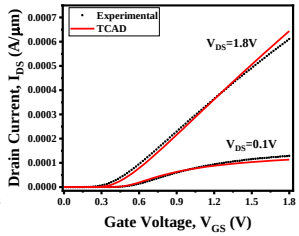
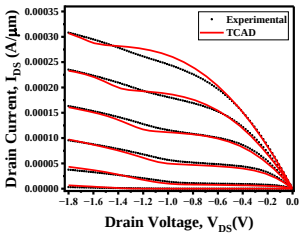


Fig.1(a) Calibration of n-PDSOI MOSFET



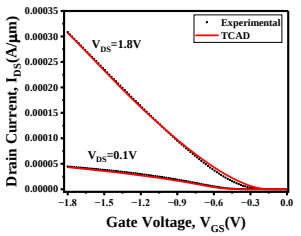
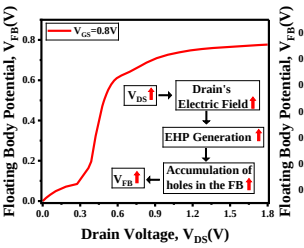


Fig.1(b) Calibration of p-PDSOI MOSFET



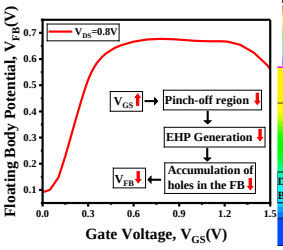


Fig.2(a) FB Potential versus V_{DS} & V_{GS}

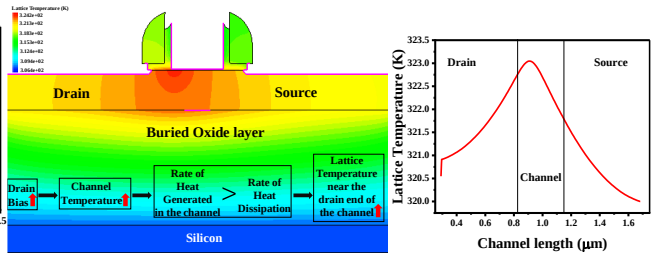


Fig.2(b) Analysis of Self-Heating Effect

$$\frac{I_{ii}}{I_{DS_o}} \propto exp\left(\frac{-\left(E_g - q(V_{DS} - V_{D_{sat}})\right)}{kT}\right)$$

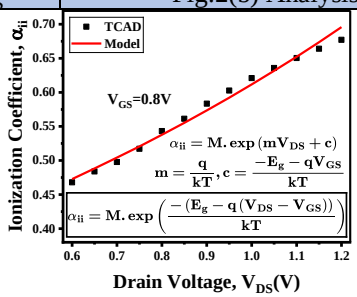
I_{ii} = Ionization current.

I_{DS_o} = Drain current without II.

$$\alpha_{ii} = \left\{A.\ exp\left(\frac{qV_{th}}{kT}\right).exp\left(\frac{-(E_g - q(V_{DS} - V_{GS}))}{kT}\right)\right\}$$

$$\alpha_{ii} = \left\{M.exp\left(\frac{-(E_g - q(V_{DS} - V_{GS}))}{kT}\right)\right\}$$

Fig.3(a) Modeling of Ionization coefficient



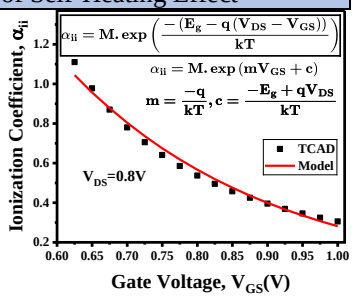


Fig.3(b) Ionization Coefficient (α_{ii}) versus V_{DS} & V_{GS}

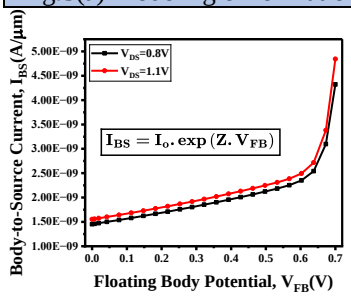


Fig.4 I_{BS} versus V_{FB}

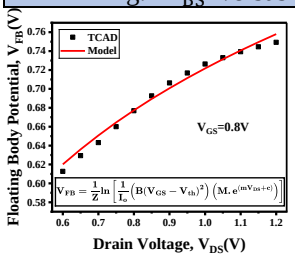
$$I_0 exp^{[Z.V_{FB}]} = \alpha.I_{DS_0}$$

$$I_0 exp^{[Z.V_{FB}]} = \{[M.exp^{[mV_{DS}+c]}].[(0.5.\mu_n C_{ox}(W/L))((V_{GS} - V_{th})^2)]\}$$

$$V_{FB} = \left\{\left(\frac{1}{Z}\right) ln\left[\left(\frac{1}{I_0}\right)(B(V_{GS} - V_{th})^2)(M.exp^{[mV_{DS}+c]})\right]\right\}$$

where Z, I_0, m, M, c are the fitting parameters

Fig.5(a) Expression of Floating Body (FB) model



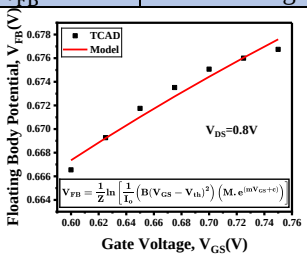
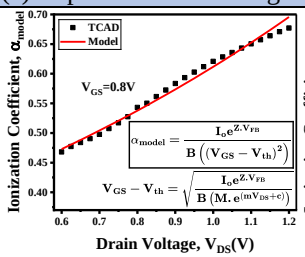


Fig.5(b) V_{FB} versus V_{DS} & V_{GS}



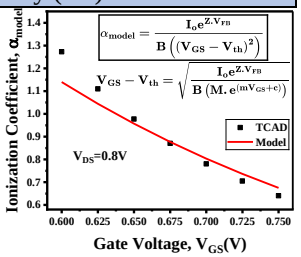
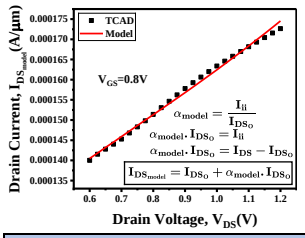


Fig.6(a) α_{model} versus V_{DS} & V_{GS}



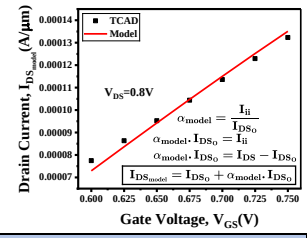


Fig.6(b) $I_{DS_{model}}$ versus V_{DS} & V_{GS}

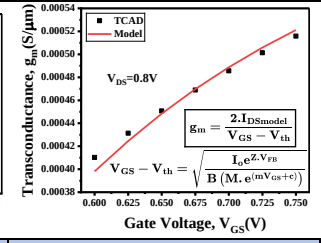


Fig.7(a) g_m versus V_{GS}

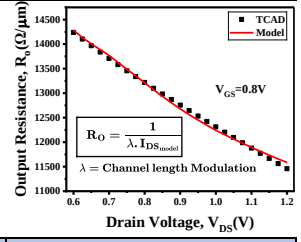


Fig.7(b) Ro versus V_{DS}

A Super low power Frequency Multiplier covering 6 to 9 GHz in 22-nm CMOS-FDSOI Technology

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Abstract: In the recent times, with the growing success of 5G , there has been increase in the demand of frequency spectrum in 22-28 GHz frequency band. The application of that frequency band covered in this paper, is mainly for medical, communication applications [1].

In this paper, a novel low power frequency multiplier is presented which can be used for the data communication. This circuit is implemented in 22-nm FDSOI technology from GlobalFoundries.
It consists of three stages: Amplification and nonlinear combiner, LC filter and gain part [2],[3].

The most critical and complex part of it is the amplifier stage with the impedance transformation using forward feedback path. The middle stage consists of high pass LC filter to suppress the first 2 harmonics.

The 3rd stage consists of the output pad-buffer designed at 50Ω load. The modelling of the width and length of CMOS-transistors is done using gm/Id technique. Here our aim was to optimize the power consumption, bandwidth and overall area of the chip. In addition to dc-analysis, transient simulation gave us useful information on behavior in time domain.

Design Description:

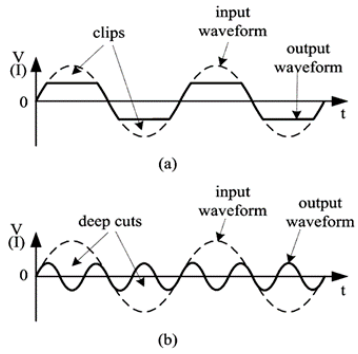

Figure 1(a): Input/output waveform with the clips, Figure 2(b): “Deep cut” on the input at non-linear combiner stage

This Third-Harmonic-Enhanced technique reach form of the signal envelope [4]. Contrary to the usage of the “oversteering” elements, where only the peak parts are eliminated, to reach the rectangle pulse at the output, this method saves us the deployment of the filters in this stage. Inverted signal comes to the nonlinear combiner, consisting of the two PFETs and two NFETs, where this “deep cut” occurs (Fig. 1).

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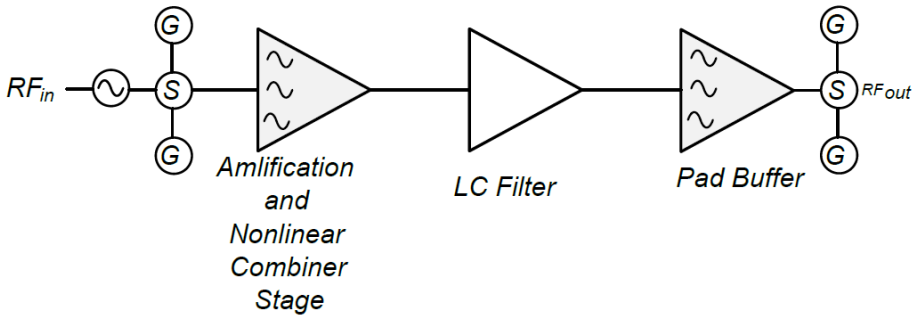

Figure 2(a): Frequency Tripler block diagram

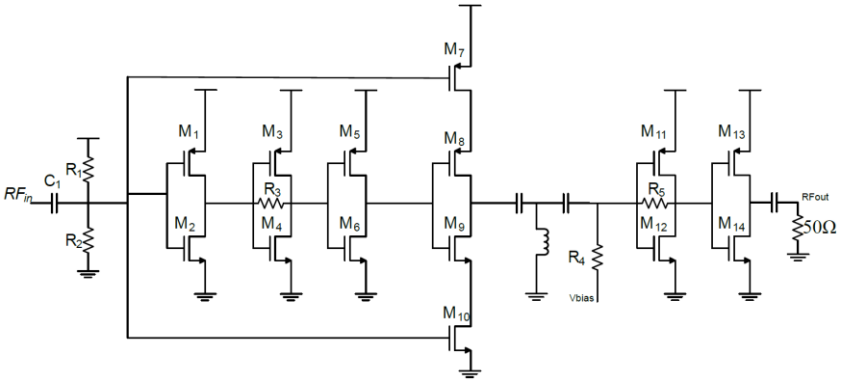

Figure 2(b): Schematic details of the designed blocks

RF_{in} is the input LO signal, interfaced to the three-stage amplifier followed by a nonlinear combiner. The advantage of 3 stage amplifier is signal stability provided by impedance transformation. A high pass filter suppresses the first two harmonics, and an output gain stage drives the signal at 50 Ω, shown in Fig. 2(b).

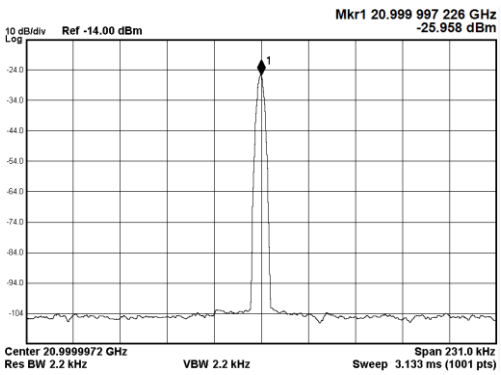

Figure 3: Output for RF_{in} of 7 GHz

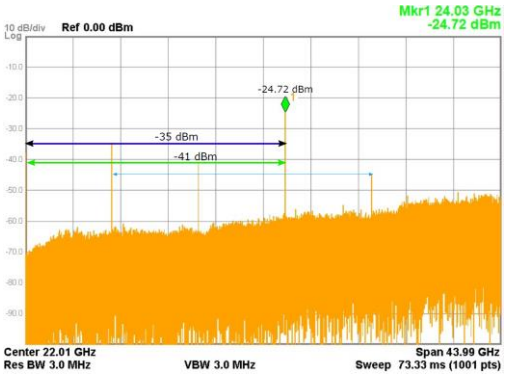

Figure 4: Harmonics measured at 24 GHz

Input frequency [GHz]	DC-Current Consumption [mA]	Input Power [dBm]	Output Frequency [GHz]	Output Power [dBm]
6-9	9	0	18-27	-24

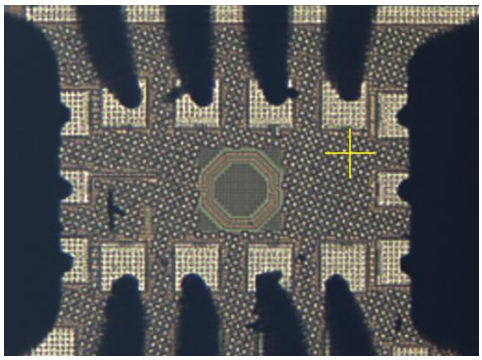

Figure 5: Die photo.

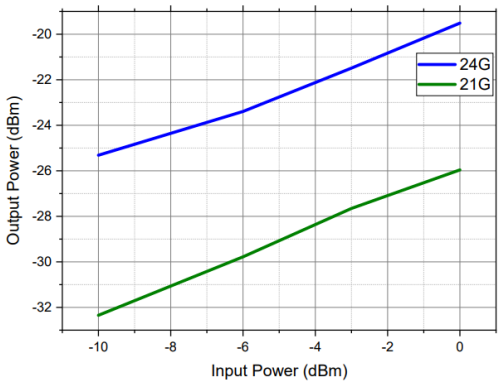

Figure 6: Input vs Output Power at 7/8 GHz RF_{in}

Results and Discussion:

Our chip demonstrates that the frequency Tripler generates an output frequency from 18 GHz to 27 GHz, shown in the Fig. 3. The other important aspect of our design is the suppression of the first two harmonics, shown in Fig. 4. Simulation and measurement results are in line and important parameters are presented in Table 1. Fig. 6. describes the variation in output power for the input frequency of 7 GHz. The measured cable loss and probe loss is 10 dBm.

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TID aware Efficient Standard Cell Characterization and its Application on the Path level Timing Performance of the Digital Circuits

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In the standard cell library characterization, extensive SPICE simulations are performed to calculate the delay of a standard cell as a function of input transition time (T_R) and load capacitance (C_L) [1]. Total Ionizing Dose (TID) caused by radiation exposure, such as in space or radiation environments, affects the timing performance of various standard cells (logic gates). TID-induced charge buildup in gate oxide can alter transistor characteristics, leading to changes in the delay of a standard cell [2]. This change in the delay affects the digital timing closure and the reliability of a random logic path. From the best-of-literature survey, none of the research groups has addressed this issue. In this article, we propose a TID-aware, efficient standard cell characterization to generate a standard liberty format to predict the overall timing closure of a design in the presence of TID. We execute this task with the help of the following steps:

1. We calibrate our 32 nm Sentaurus TCAD setup with the experimental data present in [3], and the results are shown in Fig 1.
2. We use [2, 4, 5] to estimate the value of TID, which alters the transistor characteristics.
3. We use the estimated value of TID from Step '2' in the 32 nm calibrated TCAD setup to estimate the change in transistor parameters such as threshold voltage (V_T) and leakage current in pre-radiation and post-radiation conditions using I_D-V_{GS} characteristics as shown in Fig. (2)-(4).
4. We use the estimated value of V_T as a function of TID radiation and modify the BSIM3 model parameters to incorporate the impact of TID on the delay of a standard cell as a function of T_R and C_L.
5. We extend our earlier work in [1, 6] to develop device-level variation (including TID) aware timing models of the standard cells. The large range of T_R and C_L required to generate standard cell library data with the help of two models:

   Model 1: $T_{delay} = A_1 T_R + A_2 C_L + A_3$ for small T_R and large C_L range (1)

   Model 2: $T_{delay} = A_4 T_R + A_5 \sqrt{T_R}$ for large T_R and small C_L range (2)
6. With very few SPICE simulations using Step '5', we extract model coefficients to reduce the SPICE simulation overhead required to generate TID-aware standard cell library data, and the results are shown in Fig. (5)-(8).
7. Furthermore, the impact of TID can be included to predict the impact of TID on the path level timing performance of digital circuits as shown in Table 1.

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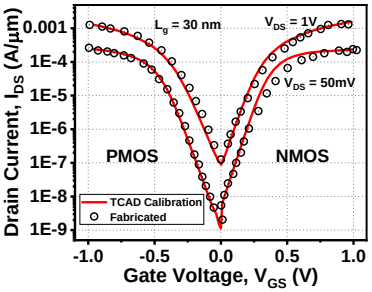

Fig. 1. Calibration of the TCAD models with fabricated data for Lg = 30 nm.

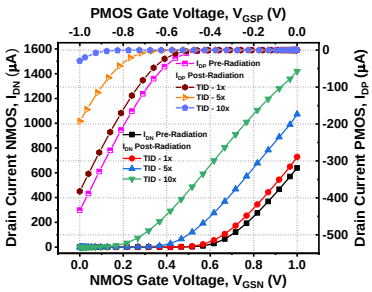

Fig. 2. Pre and Post Radiation I_D-V_{GS} characteristics of calibrated NMOS and PMOS.

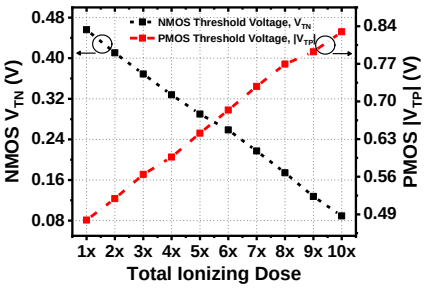

Fig. 3. Impact of TID on V_T of calibrated NMOS and PMOS devices.

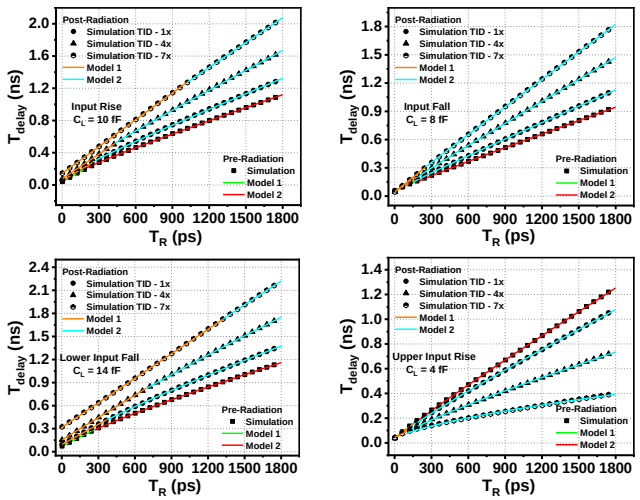

Fig. 4. Prediction of pre-radiation and post-radiation delay of: (a) Inverter (b) Buffer (c) NOR (d) AND.

Benchmark Circuits	Delay (ps) Pre-Radiation		Delay (ps) Post-Radiation					
			TID = 1x		TID = 4x		TID = 7x	
T_R = 1050 ps	Simulation	Model	Simulation	Model	Simulation	Model	Simulation	Model
c432	538.560	539.296	604.910	605.600	723.210	723.869	843.990	844.620
c499	624.850	626.751	575.740	577.637	458.320	460.397	348.810	351.425
c1355	618.310	620.026	569.570	571.313	452.950	455.003	343.550	346.338
c1908	588.230	589.157	531.700	532.728	412.430	413.578	295.540	296.882
b74181	625.560	628.216	574.770	577.502	455.660	458.683	344.830	348.898
b74182	620.360	623.409	564.980	568.220	444.560	448.133	331.220	335.907
b74283	679.950	687.523	629.120	636.911	508.550	516.411	403.910	413.409

Fig. 5. Prediction of pre-radiation and post-radiation delay for different benchmark circuits.

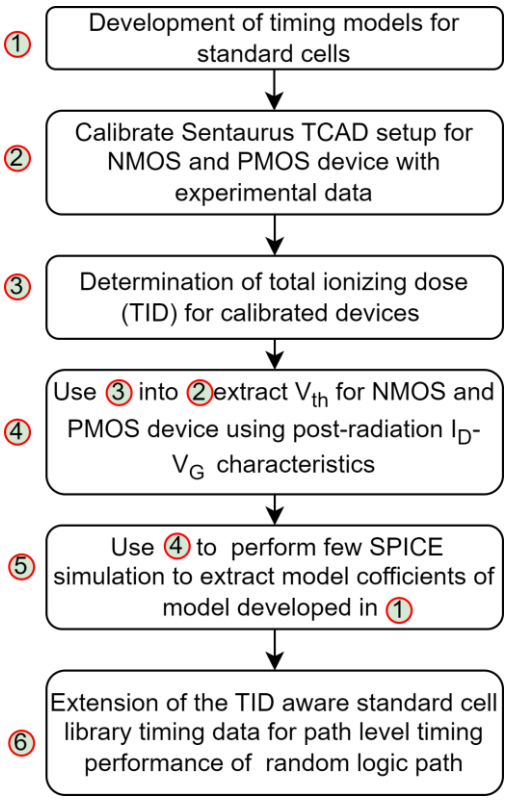

Fig. 6. Developed approach for TID aware path level timing perfroamnce of random logic path.

Switching phenomena in $CdIn_2S_4$-based neuromorphic structures

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Cadmium-indium sulfide ($CdIn_2S_4$ – abbr. C24) is a widely studied n-type chalcogenide semiconductor with a spinel structure, primarily researched for its applications in photocatalysis [1] and photovoltaics [2]. Past investigations have revealed its photosensitive nature, along with distinctive memristive properties characterized by resistive switching and memory effects [3].

In this study, we present the first experimental device utilizing $CdIn_2S_4$ as the active layer for neuromorphic applications. Polycrystalline $CdIn_2S_4$ thin films were deposited via physical vapor deposition on SLG/Mo substrates. By controlling the deposition temperature, we managed the stoichiometry of the layer. These films were coupled with a polycrystalline ZnO:Al layer acting as a transparent electrode, with aluminum electrodes completing the device structure (Fig. 1). Our devices exhibited distinct switching processes, notably transitioning between forward and backward diode regimes (Fig. 2,3), indicating reversible changes in barrier heights at different junctions. These transitions were not abrupt, hinting at a complex mechanism possibly involving defect occupancy modulation or ionic migration. Measurements revealed a significant increase in forward voltage at regular stoichiometry, suggesting Fermi level re-pinning effects (Fig. 4). A proposed band diagram (Fig. 5) illustrates potential mechanisms underlying the observed hysteresis, although precise mechanisms remain under investigation. Moreover, post-deposition treatments were employed to manipulate native defects in the CdIn2S4 layers, highlighting their influence on device behavior. These efforts pave the way for constructing novel memristive devices, including all-optically controlled variants, leveraging the unique optoelectronic properties and metastable defects of $CdIn_2S_4$ [4].

This work marks an initial exploration into utilizing $CdIn_2S_4$ for neuromorphic devices, offering promising avenues for future research and technological advancements.

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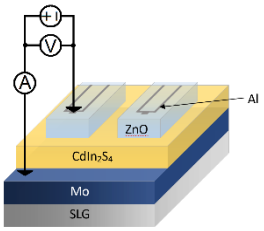

Figure 1 Schematic illustration of the Mo/C24/ZnO/Al junction structure.

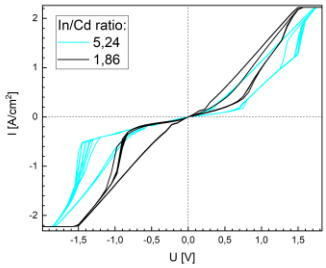

Figure 2 IV characteristics of devices with two distinct cadmium content. Ten consecutive sweeps showing repetitiveness and/or equilibration process.

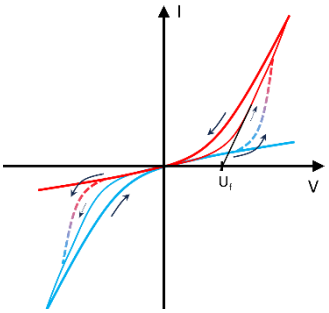

Figure 3 Schematic representation of the switching behavior. Red – device set to forward diode regime; blue – device set to backward diode regime. U_f – forward voltage.

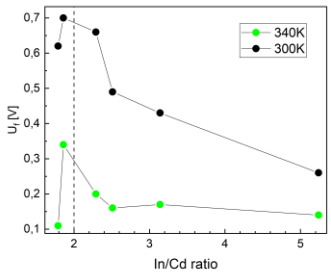

Figure 4 Stoichiometry dependence of forward voltage U_f (at Mo/C24) at two working temperatures.

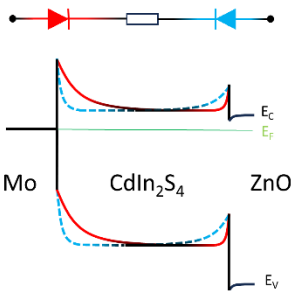

Figure 5 Proposed band diagram for the structure. Red – device set to forward diode regime; blue – device switched to backward diode regime.

Integration of membrane waveguide lasers

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Vertical external-cavity surface-emitting lasers (VECSELs) are semiconductor structures with an active region consisting of multiple quantum wells (QWs) sandwiched between air and a distributed Bragg reflector (DBR). Membrane external-cavity surface-emitting lasers (MECSELs) were recently developed [1] to demonstrate lasing without a DBR. MECSELs exhibit edge emitting lasing because the excitonic dipole in a semiconductor QW lies on the plane perpendicular to the growth direction and parallel to the surface of the epitaxial substrate [2]. In this work, we investigate the laser characteristics of the in-plane lasing effect. We present optically pumped membrane quantum well lasers (MQWLs), lasing in-plane as a single laser without the use of an external cavity. The absence of a DBR offers fast and improved quality growth, flexible wavelength design, and possibility of integration on silica on silicon. High index contrast between the membrane and substrate ensures a high overlap of the guided mode with the QW gain region.

In-plane lasing is achieved by delivering non-resonant $808\,nm$ light on top of the $1.57\,\mu m$ thick membrane sample, consisting of ten $10\,nm$ thick $In_{0.13}Ga_{0.87}As$/ $GaAs_{0.94}P_{0.06}$ QWs on a SiO_2/Si substrate, which in turn emits at $\sim 1\,\mu m$. Emitted light is collected, and then split and sent into the real and reciprocal space paths. Laser characteristics were investigated with real and reciprocal space images (Fig. 1). Real space images show the membrane's top view, fluorescence from the whole pumped region and laser spots at the end facets. Reciprocal space images display the interference patterns formed by the laser spots and strongly indicate lasing. The laser emits $1013.47\,nm$ at $14\,℃$ and $385.2\,mW$ pump power. As temperature rises, the laser wavelength increases by $(7.92 \pm 0.04) \times 10^{-2}\,nm.℃^{-1}$ from $12\,℃$ to $17.7\,℃$, achieving a $0.43\,nm$ tuning range.

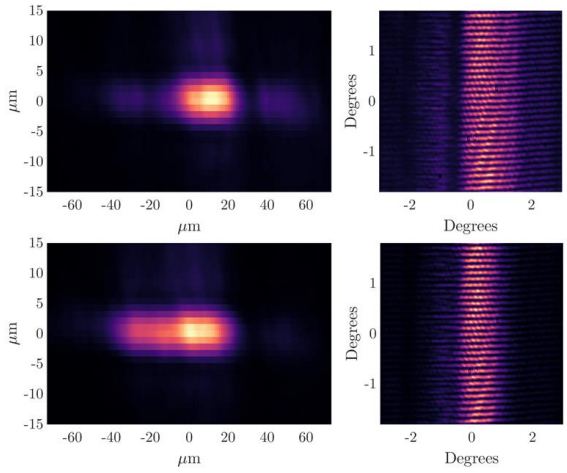

Fig. 1. Control of MQWL spatial mode width and corresponding interference pattern [2].

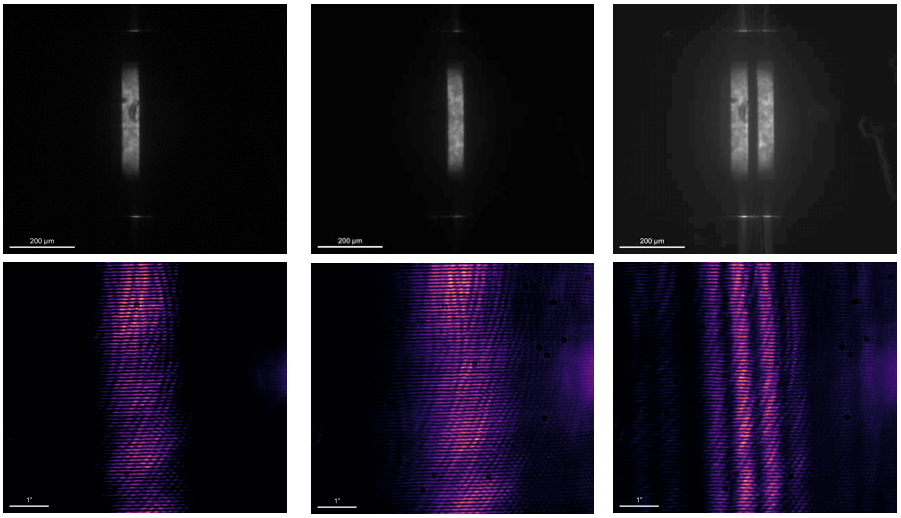

Fig. 2. Control of MQWL with DMD, creating two different lasers, on their combination the horizontal interference shows the coherence of the lasing modes.

By translating the collimation of the pump we change the pump spot's full width half maximum (FWHM), it has been shown that the laser spot width can increase by broadening the pump spot [2]. The increasing laser spot along the end facet is subjected to less diffraction resulting in a narrower interference pattern (Fig. 2).

Now we change our setup and we reflect our pump on a digital micromirror device (DMD) so we can control the shape of the illumination on the membranes and the results are shown in Fig. 3 where two stripes of pump are imaged on the membrane laser. When the two laser cavities work synchronously the interference pattern is showing that the two laser cavities work coherently and in anti-phase.

Conclusions

In-plane lasing in waveguide membrane samples by a single laser on a standard SiO_2/Si substrate is realised allowing potential on-chip integration with other photonic devices. Real and reciprocal imaging displayed lasing, with the latter being a stronger indicator due to interference between coherent light sources from the cavity's end facets while giving us information about the coherence between laser arrays [2]. In addition, spectroscopy showed that the laser emits at $1\,\mu m$ and the potential of temperature spectral tuning was demonstrated. Future work will involve slope efficiency determination, and launching on to silicon waveguide system to demonstrate coherence.

Acknowledgements

We would like to thank EPSRC for the grant EP/T001046/1.

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Assessing the Ion Sensitivity of Si_3N_4-based Feedback Field Effect Transistor Using Snap-Back Characteristics

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Abstract: We demonstrated a vertical nanowire feedback field effect transistor (FBFET) as an ion sensor in this work. The sensing mechanism of the FBFET draws upon the principles of the Gouy-Chapman-Stern layer and the site-binding model. Si_3N_4 deposited SiO_2-based insulator layer is used as a sensing layer. Sensitivity parameters are obtained from snap-back characteristics and evaluated against work function engineering variations. Varying the gate work function from 4.0eV to 4.4eV, FBFET resulted in a constant current sensitivity of 1.001 to 2.36, respectively, and a constant voltage sensitivity of 1.55 to 247.

Device Structure and TCAD setup: The cross-sectional view of the vertical nanowire FBFET considered for ion-sensing is shown in Fig. 1(a). The total transport length is assumed to be 100nm, and in the transversal direction, it measures 17nm (a ratio of 15nm/2nm for Si/insulator, respectively). TCAD models used for simulation are experimentally calibrated against [1] and are shown in Fig. 1(b). For TCAD calibration, a P^+-i-N^+ based p-type FBFET with a gate length of 0.31µm and V_{DS}=1V is considered a baseline reference. To evaluate the surface potential, a second-order gradient of surface potential and total capacitance for Si_3N_4, Souy-Chapman-Stern, and site binding model presented in [2] is used, and obtained values against bulk pH are demonstrated in Fig. 2.

Working Principle: In the equilibrium state, due to the formation of a potential barrier in channel region-1 (CH1) and CH2, free electrons from the source electrode cannot reach the drain electrode. On applying V_{DS}, the energy curve in CH2 shifts downward, but due to the presence of barrier/well, carriers from the source cannot transmit to drain; thus, FBFET remains in OFF-State (very low I_{OFF}). Applying V_{GS} decreases the barrier in CH1; therefore, electrons are transferred from the source to CH2 and accumulated. The accumulation of electrons pushes the CH2-drain region in forward bias, thus triggering the drift of holes towards CH1 (a greater decrease in the barrier in CH1); hence, a positive loop forms, and transmission occurs. A detailed insight can be found in [3]. Higher gate work function (Φ_G) increases the CH1 barrier, thus lower I_{OFF} with higher Φ_G. At V_{GS}=1V, the barrier is eliminated, resulting in a similar I_{ON} [shown in Fig. 3(b)].

Results: Fig. 4(a) shows the effect of Φ_G and bulk pH variation on the I_{DS}-V_{DS} characteristics. Higher Φ_G, elevates the barrier, thus decreasing electron drift from the source to the drain electrode resulting in lower I_{DS}. The timing behavior of the device is demonstrated in Fig. 4(b). Fig. 4(c) shows the snap-back characteristics of Si_3N_4-FBFET. At higher Φ_G's, variations in latch-up voltages differ with changes in bulk pH (latch-down voltage is constant). Constant voltage (at I_{DS} = 10^{-12}mA/µm) and constant current (at V_{DS}=0.55V) based sensitivity are shown in Fig. 4(d). Up to Φ_G=4.4eV, sensitivity increases with increase in Φ_G but decreases at Φ_G=5.0eV.

Conclusion: Due to low power operation, high switching speed, and sensitivity, the proposed Si_3N_4-based FBFET can be used for fast and reliable ion-sensing.

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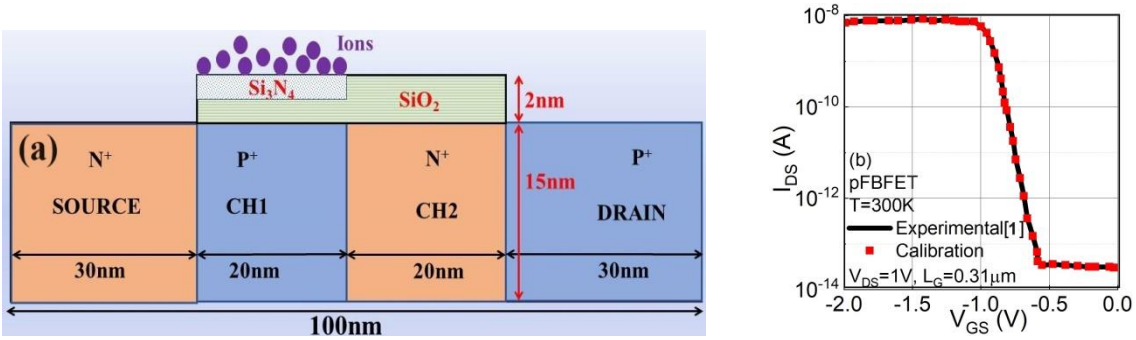

Fig. 1. (a) Planar view and physical dimensions of the investigated FBFET, and (b) Experimental verification of models used with [1] is shown. For calibration of the models, pFBFET configuration with gate length L_G=0. 31µm and V_{DS}=1V is considered.

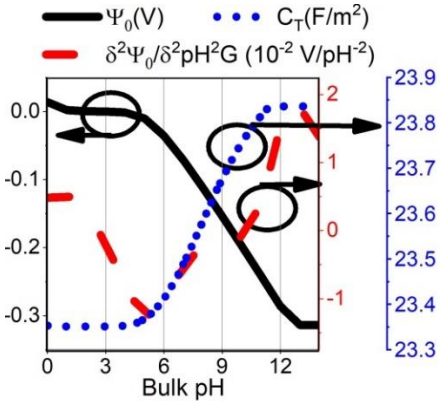

Fig. 2. Ψ_0 (left Y-axis, black), $\frac{\partial^2\psi_0}{\partial pH^2}$ (right Y-axis, red), and total capacitance (extreme right Y-axis, blue) of Si_3N_4 calculated using Gouy-Chapman-Stern layer and the site-binding model is demonstrated.

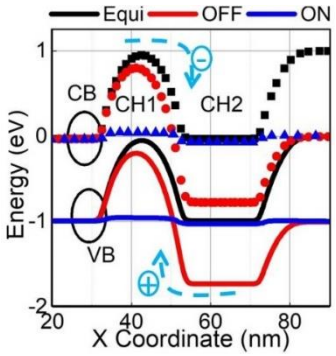

Fig.3. Energy curve of the device in Equi (black), OFF (red) and ON-State (blue) is shown.

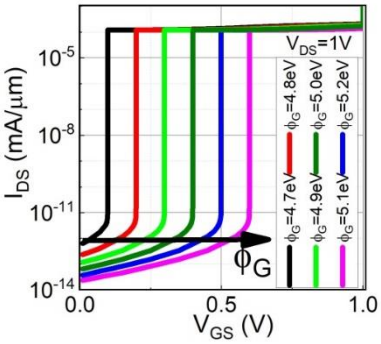

Fig. 4. I_{DS}-V_{GS} characteristics of the investigated FBFET against work function engineering at V_{DS}=1V is shown.

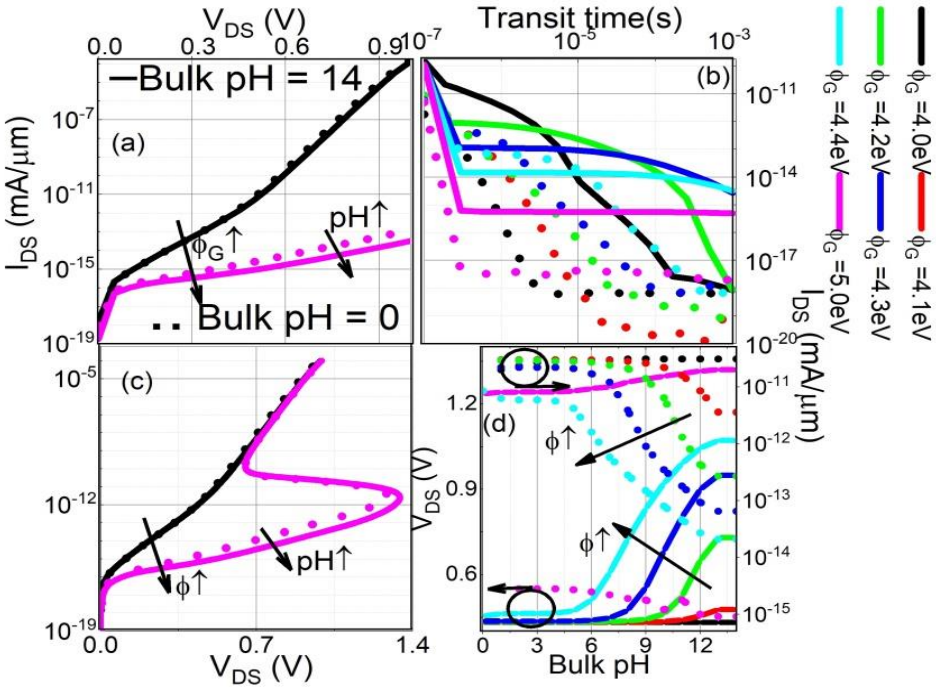

Fig. 5. The effect of variation in Φ_G and bulk pH on (a) I_{DS}-V_{DS} characteristics, (b) I_{DS}-transient time, (c) snap-back characteristics, and (d) constant current (left Y-axis) and constant current (right Y-axis) based sensitivity. The color code of variation in Φ_G is summarized in the top right corner. Bulk pH 0 and 14 are represented by dotted and solid line, respectively.

Characterization of planar CBRAM structures for RF applications

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***Abstract*—This study presents a comprehensive examination of the fabricated planar memristor devices fabricated for RF & 5G applications. Through rigorous simulation employing Synopsys' TCAD Suite and COMSOL Multiphysics, the capacitance of these devices is meticulously extracted. Under DC bias, the electric field distribution during the OFF-state is elucidated, while a uniform cylindrical filament formation is used to simulate the ON-state. The extracted device characteristics demonstrate exceptional performance, placing them in close proximity to the current state-of-the-art devices in this field. Finally, a thorough discourse is provided on strategies for enhancing the material stack of the device to achieve optimal performance.**

***Index Terms*—5G and Beyond, CBRAM, FEM, RF Circuits, S-Parameters, Tunable Circuits, Wireless Communications**

I. Introduction

The ever increasing demand for enhanced performance coupled with the need for reduced power consumption has become an overarching concern in modern electronics [1]. This necessity transcends consumer electronics and extends to pivotal sectors such as automotive technology, aerospace, military equipment, and beyond. However, the era of conventional CMOS technology, once synonymous with relentless advancement under Moore's Law, now finds itself at a juncture of diminishing returns [2], [3]. As the limitations of CMOS technology become increasingly apparent, the pursuit of alternatives heralds the dawn of a post-CMOS era. In this landscape, emerging technologies are seizing the spotlight, promising revolutionary advancements in circuit design and system architectures.

Recent strides in the telecommunications sector serve as a compelling testament to this paradigm shift. With the integration of novel devices, architectures, and materials, telecom networks are poised to transcend conventional boundaries, achieving unprecedented levels of efficiency and performance, and miniaturization [4]. Notably, the integration of memristor devices in RF applications stands at the vanguard of this technological renaissance. Leveraging the unique properties of these devices, such as non-volatility, in-memory computing, and low-power operation, researchers are pioneering novel approaches to RF circuit design, promising paradigm-shifting advancements in wireless communication systems. Furthermore, within the realm of RF memristor structures, there is a notable focus on planar architectures for fabrication methods [5]–[8]. These planar approaches have garnered attention for their advantageous trade-offs compared to traditional vertical implementations.

In this work, the planar memristor devices engineered specifically for cutting-edge RF and 5G applications are explored. Leveraging the capabilities of *Synopsys' TCAD Suite* and *COMSOL Multiphysic*s for simulation, the capacitance values are extracted and compared. Analysis under DC bias conditions illuminates the electric field distribution in the OFF-state, providing insights into device behavior under non-conductive scenarios. Conversely, the simulation of the ON-state employs a model of uniform cylindrical filament formation, offering a nuanced understanding of the conductive phase. This examination reveals the characteristics that highlight the exceptional performance and competitive positioning of this device within the field. The manuscript concludes with a discussion on strategies to refine the devices' material stack, aiming to enhance performance and functionality.

II. Device Fabrication

The investigated devices in this report are planar structures, taking inspiration for the ones described in [5], [9], featuring an air gap between the active and counter electrodes. These structures were fabricated on top of a 300nm SiO_2 layer grown by wet oxidation on a 100mm Si wafer. The active electrodes comprise a 50nm thick Ag layer, while the inert electrodes were fabricated using a Pt layer of similar thickness. The distance between the two electrodes varied from 50nm to 300nm. Fabrication of the electrodes was achieved using electron beam lithography and a metal lift-off process. Figure 1 displays top-view images of the fabricated test structures obtained from an optical microscope.

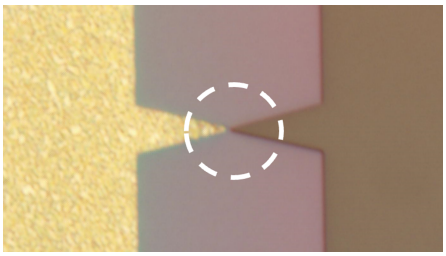

Fig. 1: Top view of the studied devices, illustrating the materials employed for fabrication. Notably, the Ag (left) and Pt (right) components, each approximately 50nm thick, are positioned atop the SiO_2 substrate, with a 100nm air-gap between the tips.

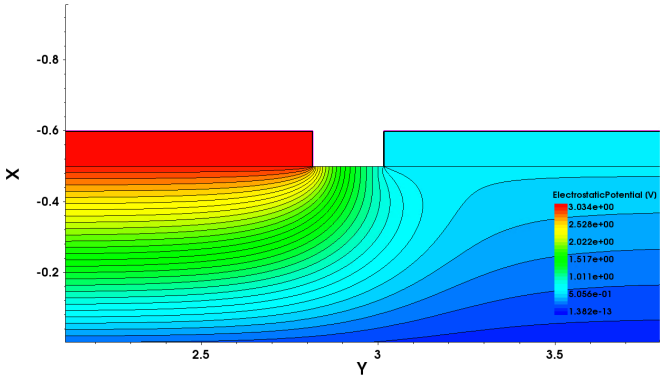

Fig. 2: Cross-sectional area of the simulated structure using Synopsys' TCAD Suite, depicting the distribution of the electrostatic potential (EP) when a positive voltage bias is applied to the Ag electrode relative to the Pt electrode.

In Figure 1 the $I-V$ characteristics of these devices are presented, indicating behavior consistent with metal ion diffusion in solid-state electrolytes. The yield of these structures was pure, as it strongly depends on the resist residuals between the electrode tips and the presence of humidity, which causes a decrease in the actual SET/RESET voltage thresholds [10].

III. Simulation Results

The devices which were studied for this work are depicted in Fig. 1 and have been previously utilized in [8]. In this work, an in-depth analysis through Finite Element Methods (FEM) will be conducted for the aforementioned devices, further backed by experimental measurements.

The simulated structure in Synopsys TCAD Suite is depicted in Fig. 2 below. In Fig. 3 the three dimensional structure simulated can be seen, along with the distribution of the electrical potential gradient.

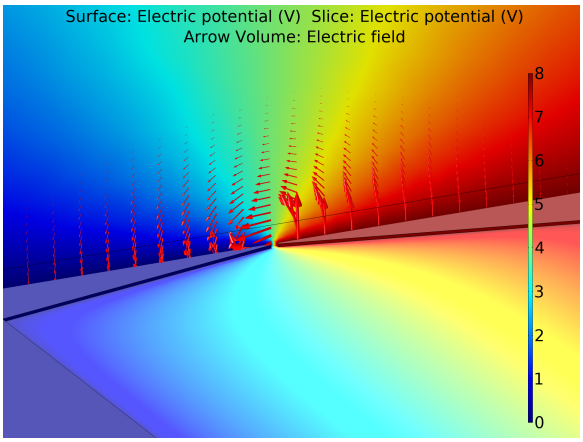

Fig. 3: Simulation of the nanostructure using *COMSOL Multiphysics*, illustrating the electric potential gradient across the structure's surface and a cut plane. The color gradient indicates the electric potential (V) from 0 (blue) to 8 (red), while the red arrows represent the direction and magnitude of the electric field induced by applying a positive voltage to the Ag electrode with respect to the Pt electrode.

IV. Conclusions

In conclusion, this study meticulously examines planar memristor devices designed for RF and 5G applications, marking a significant stride towards overcoming the limitations of conventional CMOS technology in the era of advanced telecommunications. Through detailed simulations using Synopsys' TCAD Suite and COMSOL Multiphysics, the critical capacitance values were extracted and the electric field distributions under various operational states were analyzed, showcasing the devices' exceptional performance and their competitive edge in the current technological landscape. The findings not only affirm the potential of memristor devices in enhancing wireless communication systems through improved efficiency and miniaturization but also emphasize the importance of material stack optimization. By exploring forward-looking strategies for material refinement, this work contributes to the broader endeavor of pushing the boundaries of RF circuit design and wireless communications, aligning with the ambitious goals of the post-CMOS era and beyond.

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Density Functional Analysis of Voltage Shifts through Oxide Layers in Si- and MoS_2-based FETs

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We previously showed by density functional theory how oxide layers SrO, La_2O_3, HfO_2, or Al_2O_3 could be used to adjust the electrode Fermi levels (E_F) in either n-type or p-type directions and thereby control the threshold voltages (V_{th}) in high-K/CMOS metal gate stacks, using a combination of dipole effects and band alignments. We now show that these methods can be extended to 2D TMD-channel transistors, such as MoS_2. MoS_2 inevitably contains sulfur vacancies, making it weakly n-type. We find that inserting an Al_2O_3 layer into gate stacks will shift E_F downwards and allow full inversion mode MoS_2 FETs to be regained.

When high-K oxides were introduced, different gate metals were initially suggested for n- and p-type inversion mode FETs [1], with work functions near the Si band edges for n- and p-FETs respectively (Fig. 1a). These were replaced by a single, mid-gap metal such as TiN (Ru, computationally) plus two 'dipole layers' of La_2O_3 or Al_2O_3 to shift the work functions to nearer n- or p-type Si band edges [2], as in Fig. 1(b)[3].

Here, we directly calculate the work function shifts from the band-edge energies of the oxide slab surfaces. Fig. 2 shows a schematic plot of oxide band alignments obtained by the core level or band edge methods. Given the similar band gaps of these oxides, the band alignment diagram exhibits a 'staircase' pattern of staggered band offsets. This staircase pattern of band offsets is crucial as this enables a continuous range of biasing with these oxides. We choose Al_2O_3 and Y_2O_3 as the doping layers to build multiple stacks on Si and show a real-space layer-by-layer local density of states (LDOS) in Fig. 3. It is clear that these oxides cause n- or p-type Si behaviors and the overall alignment can involve both band alignment and dipole voltage effects between interfacial charges.

We then also employ this method to vary the V_{th} shifts in 2D transition metal dichalcogenide (TMD) FETs. MoS_2 is made intrinsic n-type due to the gap states of S vacancies S_{vac}. Pop [4] noted that TMDs have not yet achieved true inversion-mode FETs, mainly due to the unpassivated dangling bonds of S_{vac}. Thus, including a V_{th} shifting layer could allow these FETs to regain full inversion mode. Thus, we first investigated a gate stack model of ideal MoS_2/HfO_2/Ru layers (Fig. 4). We then created an S vacancy in the MoS_2 to shift E_F in a n-type direction (Fig. 5a). After inserting an Al_2O_3 layer between MoS_2 and HfO_2, E_F moves downwards to the valence band maximum (VBM), showing a p-type behavior (Fig. 5b). This is because the Al_2O_3 has a lower VBM than HfO_2 (Fig. 2). Therefore, by oxide interfacial layers, the transition of MoS_2 from n-type to p-type is possible, offering the potential to achieve high-quality n- and p-FETs.

In summary, we show that dipole layers/band offest layers can be used to make MoS_2 FETs inversion mode.

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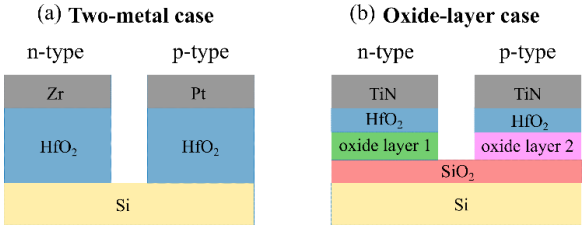

Fig. 1. Different voltage threshold settings in MOS structures (a) two-metal case with n- and p-type metal gates to shift gate voltage, (b) the oxide layer case with single TiN metal gate and an oxide layer to vary the gate voltage, V_{th}.

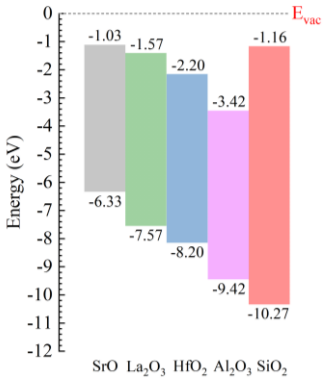

Fig. 2. Band alignments of the four oxides considered here, indicating a 'waterfall' band alignment, with staggered band offsets. E_{vac} is the vacuum level.

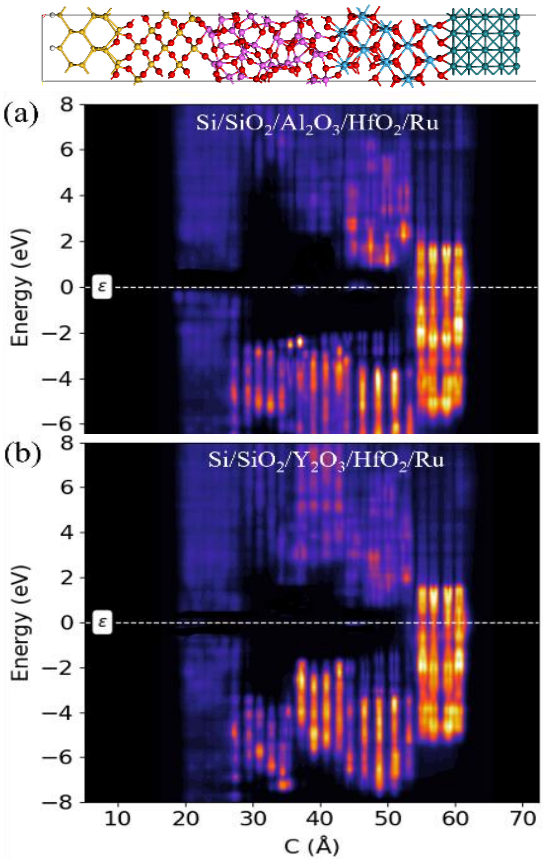

Fig. 3. GGA calculation of band edge energies vs atomic layers along the z axis for V_{th} shifting (a) p-type Al_2O_3 and (b) n-type Y_2O_3 gate stacks with Ru midgap metal, moving E_F next to (a) CBM and (b) VBM respectively. Y_2O_3 is used rather than La_2O_3 for better lattice matching.

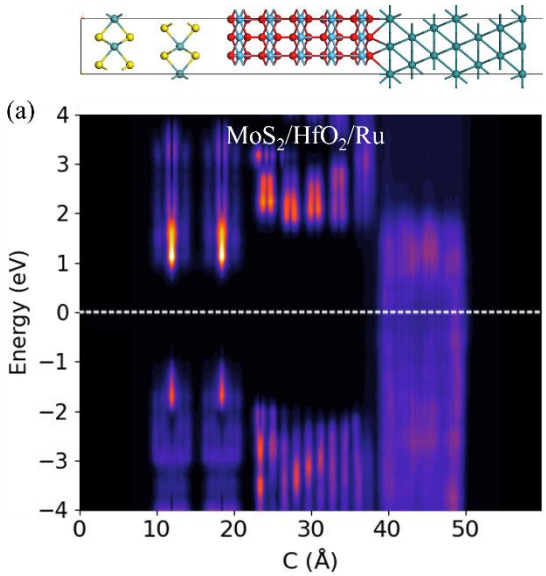

Fig. 4. Atomic model and LDOS of band edge energies vs atomic layers along the z axis for $MoS_2/HfO_2/Ru$.

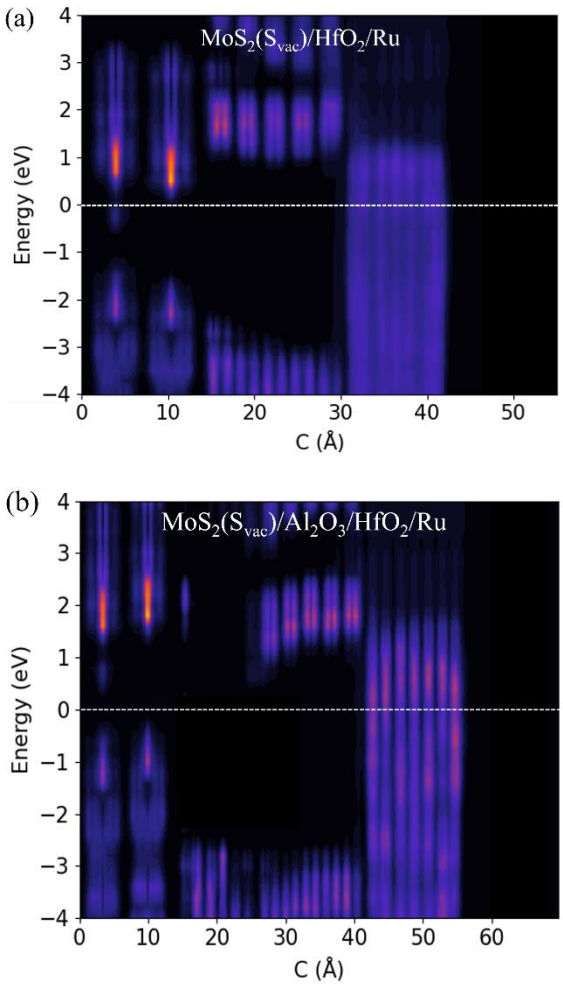

Fig. 5. GGA calculation of band edge energies vs atomic layers along the z axis for V_{th} shifting (a) $MoS_2/HfO_2/Ru$ layers with S_{vac}, and (b) $MoS_2/Al_2O_3/HfO_2/Ru$ layers with S_{vac}, moving E_F from CBM to nearer VBM, respectively.

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